JFET SPICE Modeling

The primary focus of SPICE modeling at InterFET is SPICE2 parameters which can be easily used with most industry SPICE simulators. The core reference for this material is "Semiconductor Device Modeling with SPICE" second addition, by Giuseppe Massobrio and Paolo Antognetti.

Fundamental SPICE2 JFET Parameters			
Symbol	Abbreviation	Default Value	Definition
V_{T0}	VTO	-2	Threshold Voltage
β	BETA	100u	Transconductance Parameter
λ	LAMBDA	0	Channel-Length Modulation Parameter
r_D	RD	0	Drain Parasitic Resistance
r_S	RS	0	Source Parasitic Resistance
C_{GD}	CGD	0	Initial Gate to Drain Capacitance
C_{GS}	CGS	0	Initial Gate to Source Capacitance
φ_0	PB	1	Gate-Junction Potential
F_C	FC	500m	Forward-Bias Capacitance Coefficient
I_S	IS	10f	Gate Saturation Current Parameter
a_F	AF	0	Flicker Noise Exponent on Drain Current
k_F	KF	1	Flicker Noise Coefficient on Drain Current

DC Model

The DC model parameters (V_{T0}, β, and λ) are the most crucial set of parameters needed to generate a SPICE model of a JFET. These values are expressed in SPICE2 when performing 'Id-Vds' or 'Id-Vgs' sweeps. The SPICE2 implementation of the JFET static model uses the Shichman-Hodges polynomial models to depict the Cutoff, Ohmic, and Saturation regions of JFETs as separate piecewise equations, shown in equation 1.

$$I_D = \begin{cases} 0 & (V_{GS} - V_{T0}) \leq 0 & (Zero) \\ \beta V_{DS}(2(V_{GS} - V_{T0}) - V_{DS})(1 + \lambda V_{DS}) & 0 \leq V_{DS} < (V_{GS} - V_{T0}) & (Ohmic) \\ \beta (V_{GS} - V_{T0})^2 (1 + \lambda V_{DS}) & 0 < (V_{GS} - V_{T0}) \leq V_{DS} & (Saturation) \end{cases}$$

Equation 1, SPICE equation for Drain current.

These parameters are also used to compute the Transconductance (g_m) and the Drain to Source Conductance (g_{DS}) as piecewise functions like equation 1, as shown in equations 2 and 3.

$$g_m = \begin{cases} 0 & (V_{GS} - V_{T0}) \leq 0 & (Zero) \\ 2\beta V_{DS}(1 + \lambda V_{DS}) & 0 \leq V_{DS} < (V_{GS} - V_{T0}) & (Ohmic) \\ 2\beta (1 + \lambda V_{DS})(V_{GS} - V_{T0}) & 0 < (V_{GS} - V_{T0}) \leq V_{DS} & (Saturation) \end{cases}$$

Equation 2, SPICE equation for Transconductance.

$$g_{DS} = \begin{cases} 0 & (V_{GS} - V_{T0}) \leq 0 & (Zero) \\ 2\beta (1 + 2\lambda V_{DS})(V_{GS} - V_{T0}) - \beta V_{DS}(2 + 3\lambda V_{DS}) & 0 \leq V_{DS} < (V_{GS} - V_{T0}) & (Ohmic) \\ \lambda \beta (V_{GS} - V_{T0})^2 & 0 < (V_{GS} - V_{T0}) \leq V_{DS} & (Saturation) \end{cases}$$

Equation 3, SPICE equations for Drain to Source Conductance.

Calculating these parameters for a JFET requires at least one full 'Id-Vds' sweep for that given part and is somewhat easy if r_D and r_S are assumed to be negligible. V_{T0} and β can be computed simultaneously by taking either an 'Id-Vgs' or an 'Id-Vds' sweep, taking the square-root of the drain current, and performing a linear regression from the $\sqrt{I_{DSS}}$ to some point on the sweep where the curve is still linear. The slope is equal to $\sqrt{\beta}$, and the x-intercept is V_{TO}. Figure 12 the method for calculating the values, as well as highlighting the difference between V_{T0} and $V_{GS}(OFF)$.

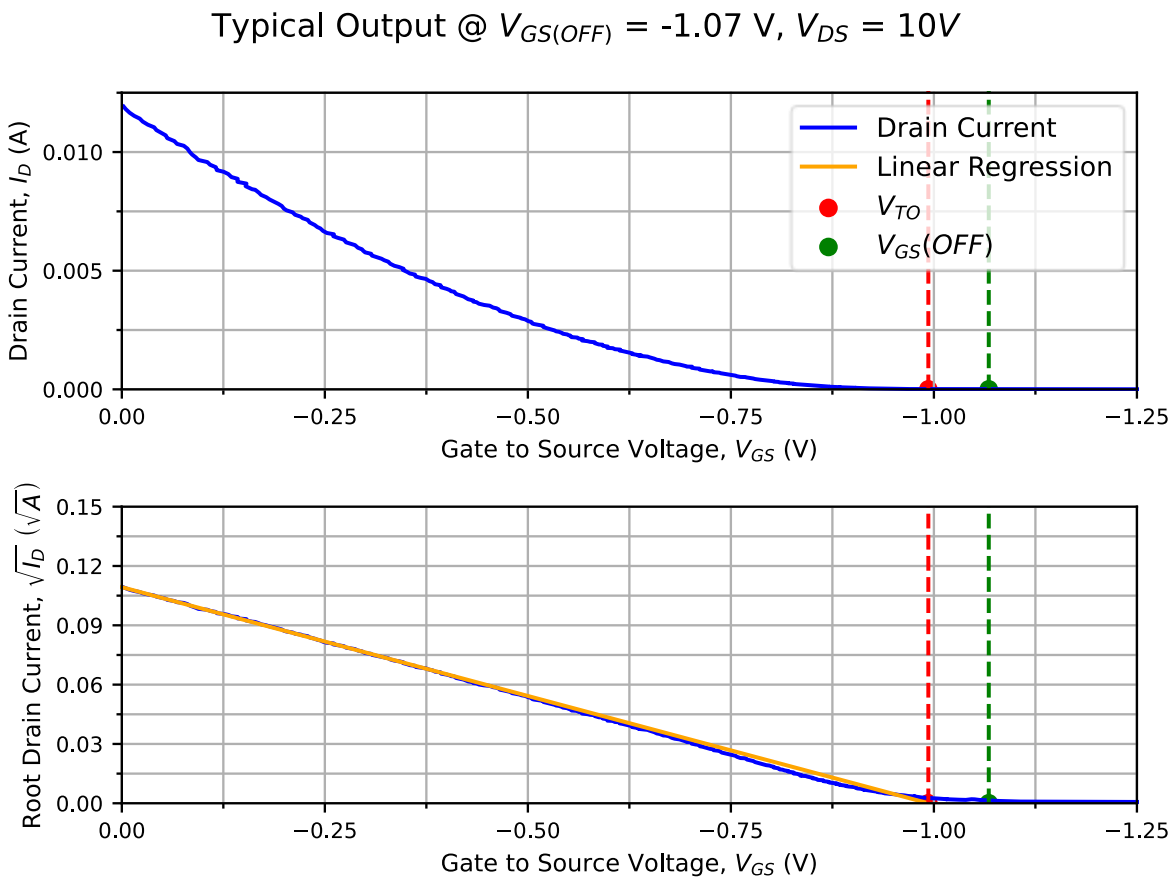

Figure 1, Using an 'Id-Vgs' sweep (N0132SL) to find a linear regression for obtaining VTO and BETA.

Computing λ is a little different and requires V_{T0} and β to be calculated first. Once V_{T0} and β are known, take an 'Id-Vds' sweep, remove all data points with $\text{abs}(V_{DS})$ less than $\text{abs}\big(V_{GS}(OFF)\big)$. I usually remove all points with $\text{abs}(V_{DS})$ below $\sim 1.2 \cdot \text{abs}\big(V_{GS}(OFF)\big)$ to ensure all remnants from the "knee" of the sweep are removed. Then perform **Equation 4** to obtain λ.

$$\lambda = \text{mean}\left(\frac{I_D(V_{DS}, V_{GS})}{\beta V_{DS}(V_{GS} - V_{TO})^2} - \frac{1}{V_{DS}}\right)$$

Equation 4, Equation for finding LAMBDA.

As a final step, you can tune β to align the SPICE curves to the real data as desired. A fast way of doing this is by recomputing the saturation region I_D using the SPICE parameters and dividing the results by the real data, averaging the result, and multiplying that by the original β to obtain a new β. For example:

$$\beta_{New} = \beta_{Old}\frac{\beta_{Old}(V_{GS} - V_{TO})^2(1 + \lambda V_{DS})}{I_D(V_{DS}, V_{GS})} \text{ for } \text{abs}(V_{DS}) > 1.2 \cdot \text{abs}\big(V_{GS}(OFF)\big)$$

Equation 5, Equation for calibrating BETA.

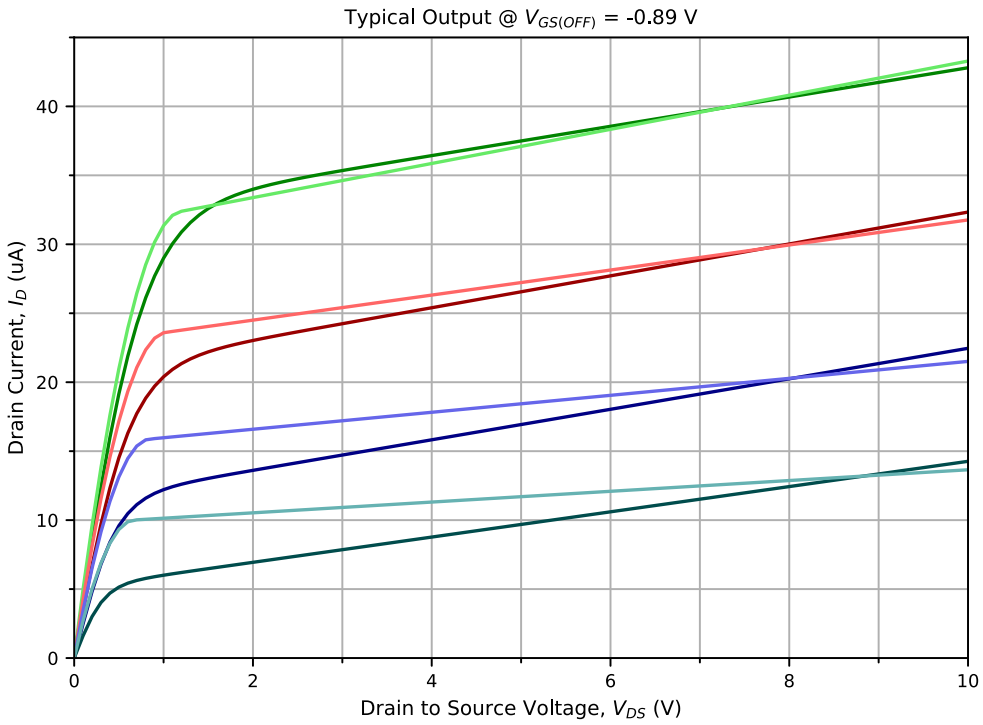

Figure 2, An 'Id-Vds' sweep (N0001SH) overlayed with a SPICE Model.

It should be noted that due to the simple nature of the SPICE2 JFET DC parameters, getting a great match won't always be possible, and sometimes the models will be poor.

Voltage Dependent Capacitors

SPICE2 handles capacitance as two components, Gate to Source Capacitance (C_{GS}) and Gate to Drain Capacitance (C_{GD}). The parameters used for this are the measured nonbiased C_{GS} and C_{GD} capacitance values, as well as the Gate-Junction Potential (φ_0) and the Forward-Bias Capacitance Coefficient (F_C). Equations 4 and 5 are for calculating the voltage-dependent capacitances as performed in SPICE2.

$$C_{GS} = \begin{cases} C_{GSi}\left(1 - \dfrac{V_{GS}}{\varphi_0}\right)^{-m} & V_{GS} \le (F_C \cdot \varphi_0) \quad (Reverse\ Capacitive) \\ \dfrac{C_{GSi}}{(1-F_C)^{1+m}}\left((1-F_C)(1+m) - \dfrac{mV_{GS}}{\varphi_0}\right) & V_{GS} > (F_C \cdot \varphi_0) \quad (Linear\ Capacitive) \end{cases}$$

Equation 6, SPICE equation for Gate to Source Capacitance.

$$C_{GD} = \begin{cases} C_{GDi}\left(1 - \dfrac{V_{GD}}{\varphi_0}\right)^{-m} & V_{GD} \le (F_C \cdot \varphi_0) \quad (Reverse\ Capacitive) \\ \dfrac{C_{GDi}}{(1-F_C)^{1+m}}\left((1-F_C)(1+m) - \dfrac{mV_{GD}}{\varphi_0}\right) & V_{GD} > (F_C \cdot \varphi_0) \quad (Linear\ Capacitive) \end{cases}$$

Equation 7, SPICE equation for Gate to Drain Capacitance.

The nonbiased C_{GS} and C_{GD} capacitances aren't necessarily always equal but can be treated as such in most cases. The nonbiased ratings for a JFET can be obtained by measuring the Reverse Transfer Capacitance (C_{rss}) at $V_{GS} = 0$ and $V_{DS} = 0$, shown in Equation 6.

$$C_i = C_{GSi} = C_{GDi} = C_{rss}(V_{GS} = 0, V_{DS} = 0)$$

Equation 8, Relation between Initial Capacitances and the Reverse Transfer Capacitance.

The Gate-Junction Potential (φ_0) of a given JFET can be computed with Equation 7 when applied to a sweep of C_{rss} data as taken in the ohmic and saturation regions of the JFET.

$$\varphi_0 = \text{MEAN}\left(\frac{V_{GS} - V_{DS}}{1 - \left(\dfrac{C_i}{C_{rss}(V_{GS}, V_{DS})}\right)^2}\right)$$

Equation 9, Equation to solve for the Gate-Junction Potential.

Gate Leakage

JFET Gate Leakage is modeled in SPICE2 similarly to that of ideal PN-Junction diodes, which additionally carries into how JFETs equivalent diodes are modeled in SPICE2. There is only one SPICE parameter involved in this calculation, being the Gate Saturation Current Parameter I_S (not to be confused with the JFET Source Current). There is also the leakage conductance SPICE value G_{Min} that can be modified separately, but unfortunately that impacts all models that utilize G_{Min} in that given simulation, including other JFETs and diodes. The default value of G_{Min} in SPICE2 is 10^{-12} Siemens.

The leakage (and overall diode behavior) is modeled as two diodes, Gate to Drain and Gate to Source. The equations for the currents traveling through the diodes is shown in **Equations 8-9**. When a JFET is configured as a two-terminal diode, either of these equations can be used if the equation is doubled and V_{GD} or V_{GS} are treated as V_D (the voltage applied to the diode). Note that $\frac{k_B}{q} = 8.617333 \cdot 10^{-5}\ eV/°K$.

$$I_{GD} = \begin{cases} -I_S + V_{GD}G_{Min} & V_{GD} \leq -5\dfrac{k_BT}{q} \quad (Linear\ Leakage) \\ I_S\left(e^{V_{GD}\left(\frac{k_BT}{q}\right)^{-1}} - 1\right) + V_{GD}G_{Min} & V_{GD} > -5\dfrac{k_BT}{q} \quad (Exponential\ Leakage) \end{cases}$$

Equation 10, SPICE equation for the Gate to Drain Leakage Current.

$$I_{GS} = \begin{cases} -I_S + V_{GS}G_{Min} & V_{GS} \leq -5\dfrac{k_BT}{q} \quad (Linear\ Leakage) \\ I_S\left(e^{V_{GS}\left(\frac{k_BT}{q}\right)^{-1}} - 1\right) + V_{GS}G_{Min} & V_{GS} > -5\dfrac{k_BT}{q} \quad (Exponential\ Leakage) \end{cases}$$

Equation 11, SPICE equation for the Gate to Source Leakage Current.

Since the Forward-Bias Voltage (V_{FB}) of the diodes isn't directly controllable, a compromise may have to be made between choosing an accurate gate leakage current and accurate V_{FB}. Additionally, it should be noted that the diode breakdown voltage and current is not included in the JFET diode model. **Figure 14** shows a diode characteristic of an example JFET using the SPICE2 equations using an N-channel J109.

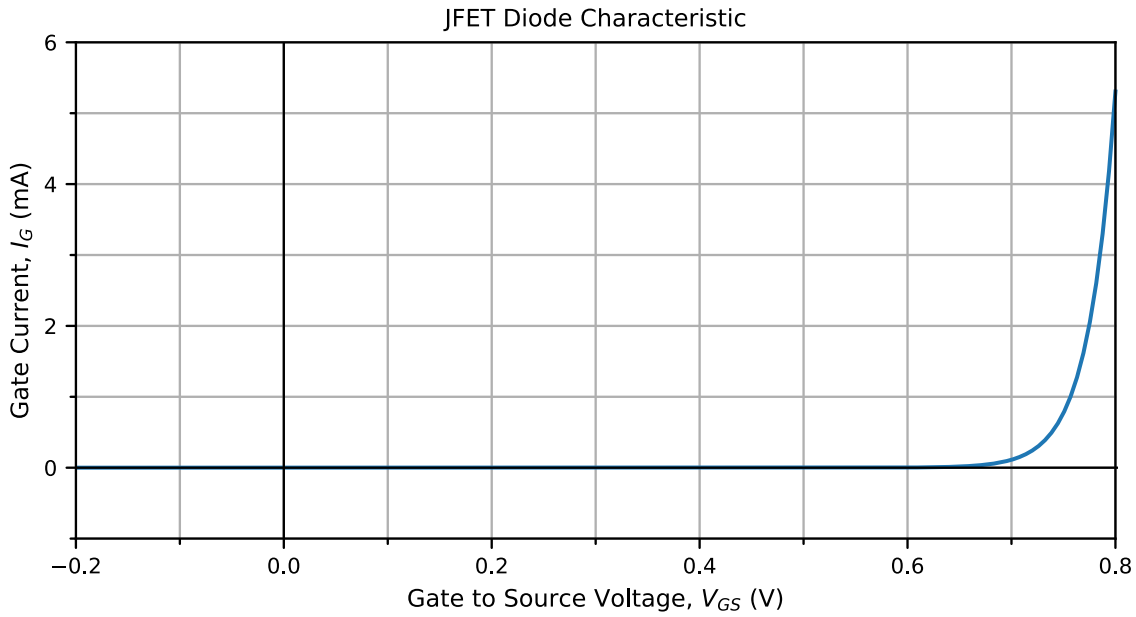

Figure 3, An 'Ig-Vgs' sweep (N0450SL) showing the JFET diode behavior in SPICE2.

The I_S parameter can be computed alongside G_{Min} (default $G_{Min} = 10^{-12}$ Siemens) or be computed independently. By shorting the Source and Drain pins of the FET and reverse biased the FET, a reverse-bias diode characteristic will be formed, and can be used in the following equations for computation:

For the I_S parameter:

$$I_S = V_D G_{Min} - I_G(V_D)$$

Equation 12, Equation for computing Gate Saturation Current Parameter.

For both the I_S and G_{Min} parameters, a full reverse-bias sweep will be needed, and to perform a linear regression to obtain a slope (m_g) and an intercept (b_g):

$$I_S = -b_g \quad G_{Min} = m_g$$

Equation 13, Equation for computing Gate Saturation Current Parameter and the Leakage Conductance.

Parasitic Resistances

All real JFETs exhibit parasitic resistances to varying extents, because of bond wires, semiconductor resistances, lead resistances, etc.. Working with parasitic resistances is tricky, because the parasitic resistances are not possible to model with a single equation and instead need to be simulated.

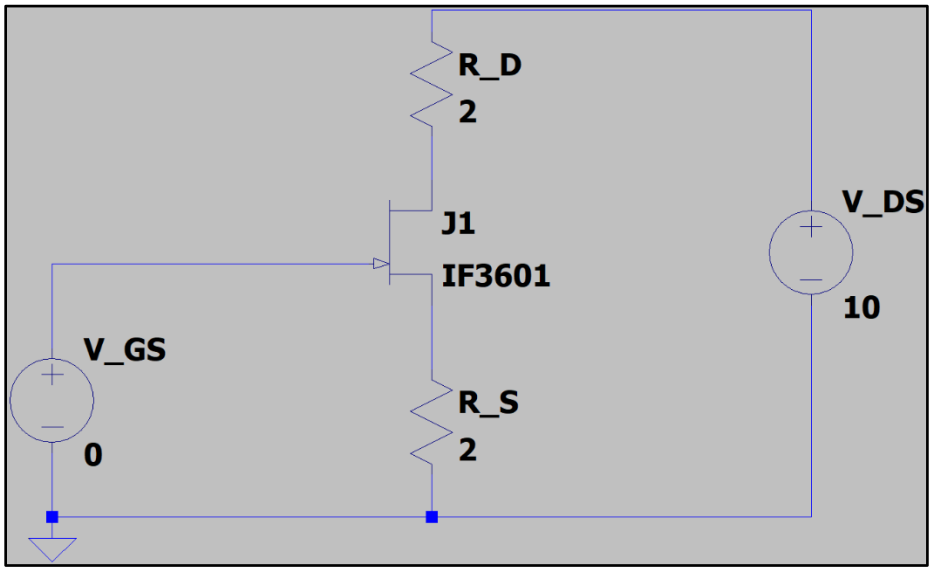

Figure 4, A JFET model showing parasitic resistances externally. Schematic produced using LTSpice.

Even though the parasitic resistances are typically less than 10 Ohms, the impact of these resistances can be significant, especially on parts with higher I_{DSS}. **Figures 16-18** show the impact of parasitic resistances on a high-current JFET, note the impact of r_D on the observed knee position and the impact of r_S on I_{DSS}. There may be a way of determining the parasitic resistances if $r_D \approx r_S$ that involves performing a few 'Vgs-Id' sweep that includes a slightly positive V_{GS} to counteract the effect of r_S.

It should be noted that the parasitic resistances impact the large signal, small signal, and noise behavior of a JFET in SPICE2. As a result, modeling the parasitic resistances with precision and accuracy is a critical task.

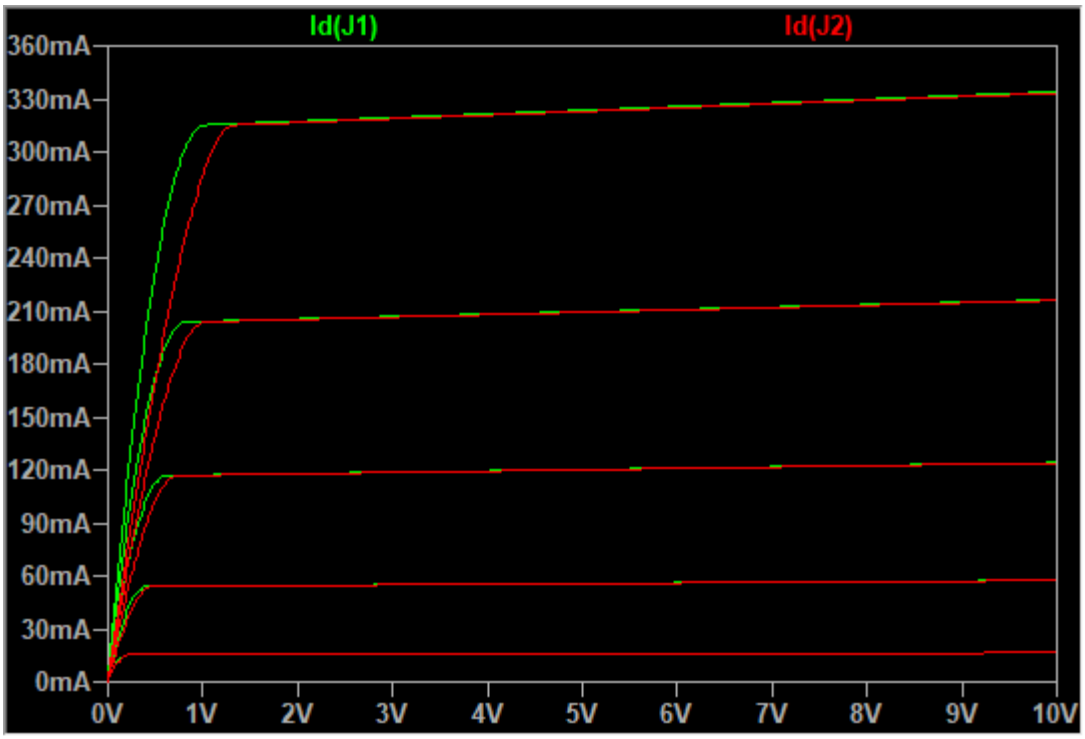

Figure 5, A comparative simulation of an IF3601 with no parasitic resistance (green) and with a 1 Ohm drain resistance (red). Simulated using LTSpice.

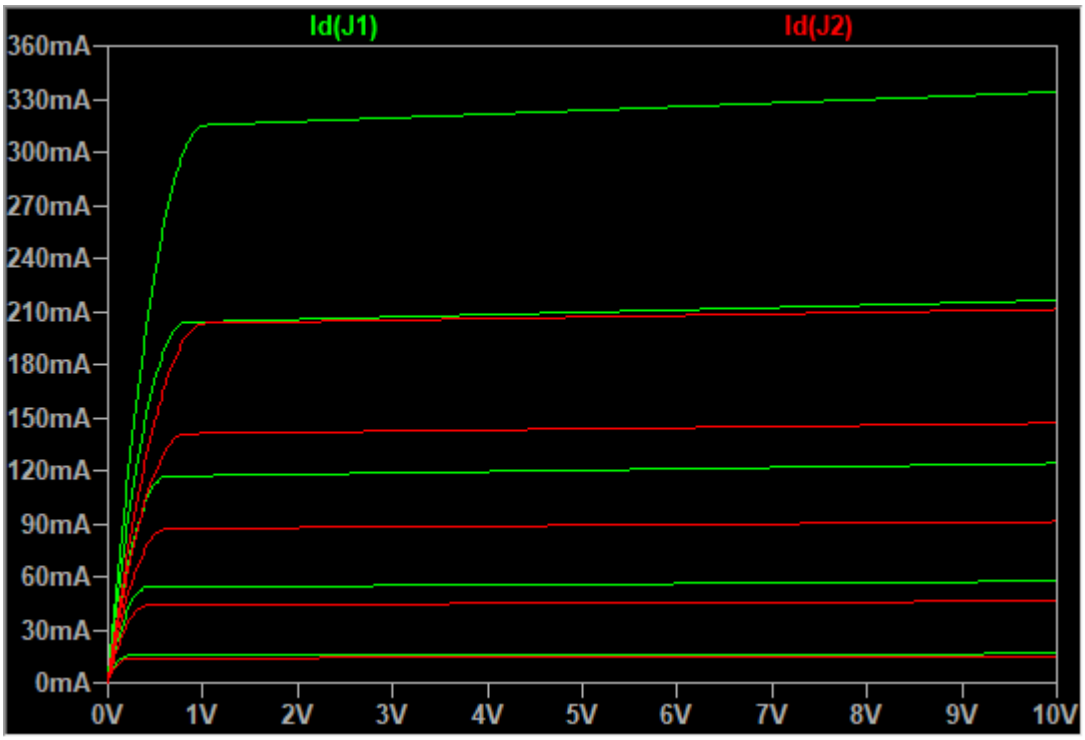

Figure 6, A comparative simulation of an IF3601 with no parasitic resistance (green) and with a 1 Ohm source resistance (red). Simulated using LTSpice.

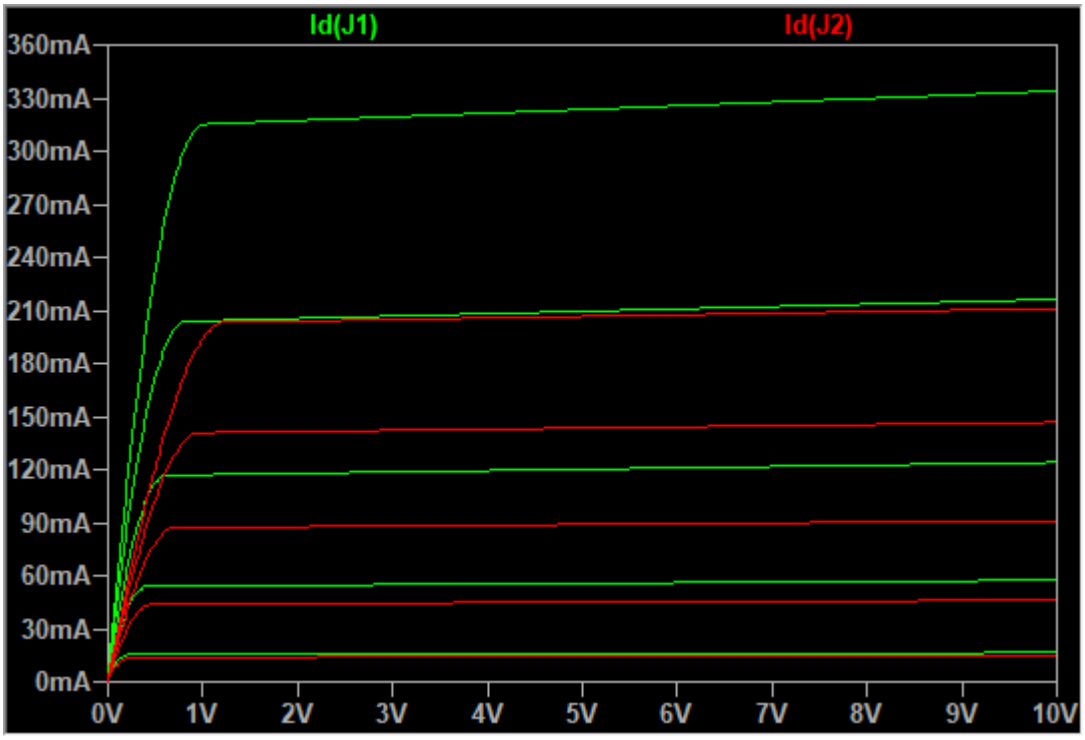

Figure 7, A comparative simulation of an IF3601 with no parasitic resistance (green) and with 1 Ohm drain and source resistances (red). Simulated using LTSpice.

Noise Equations and Approximations

JFET noise in SPICE is modeled as current sources in parallel to the channel and the drain and source parasitic resistances, with an equivalent noise model shown below:

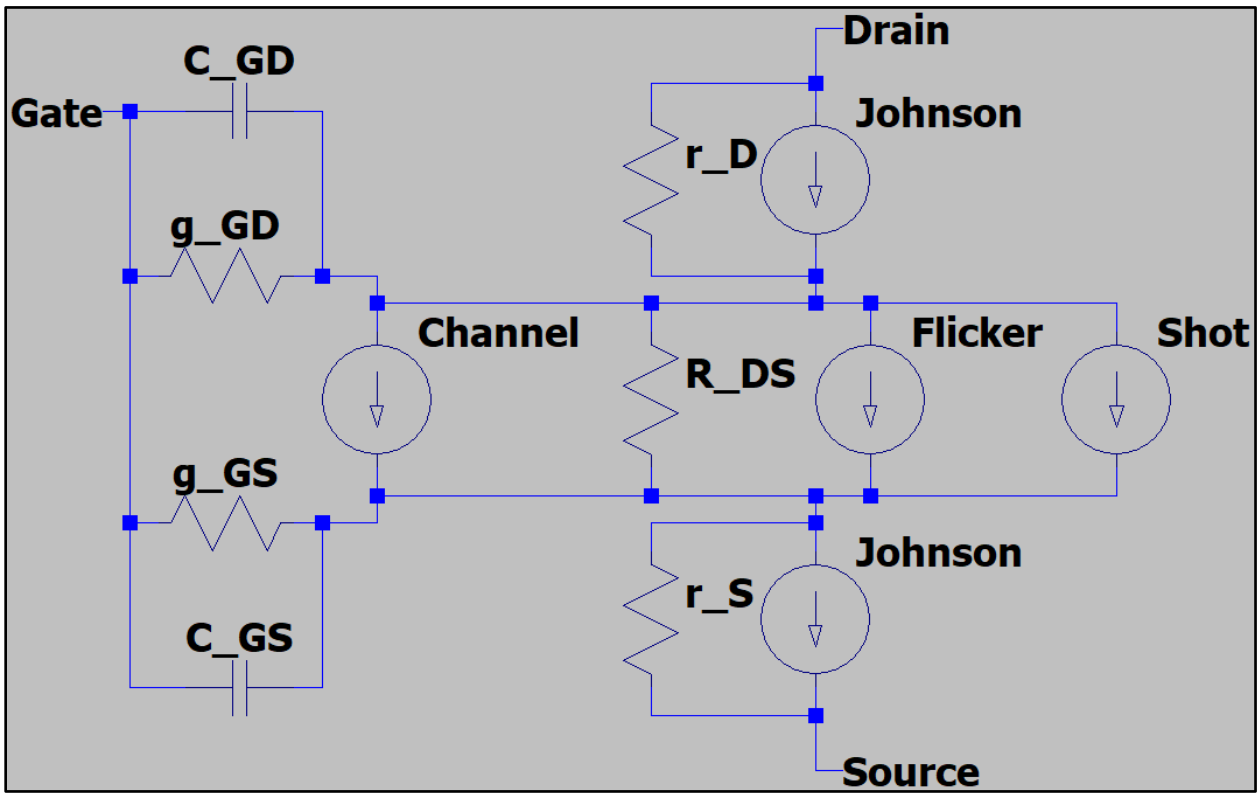

Figure 8, An equivalent small-signal model for depicting SPICE2 JFET noise current sources.

The names of each of the current sources shown depict their noise component, excluding the current source labeled “Channel,” which is a non-noise current source for depicting the small-signal current traveling through the JFET. Then the question becomes, what are Flicker, Shot, and Johnson noise? It is worth noting that $k_B = 1.380649 \cdot 10^{-23}\, J/°K$ in this section.

Flicker noise is a noise contribution with the cause not fully understood, acting on the device channel. It is the only noise contribution with SPICE parameters exclusively for this function, A_F and K_F. This noise source is impacted by the drain current and decays inversely with frequency, because of this, it is most prominent in lower frequencies [2].

$$N_{Flicker}\left(\overline{A^2}\right) = \frac{K_F {I_D}^{A_F}}{f}\Delta f$$

Equation 14, SPICE equation for the Channel Flicker Noise contribution.

Shot noise (also known as Poisson) noise is another contribution induced on the device channel. This component is caused by the discrete and chaotic behavior of moving electrical charges. This noise source is impacted by the junction temperature and the transconductance of the device at any given time. This component is present and uniform across all frequencies [2].

$$N_{Shot}\left(\overline{A^2}\right) = \frac{8k_B T g_m}{3}\Delta f$$

Equation 15, SPICE equations for the Channel Flicker and Shot Noise contributions.

Johnson (also known as Thermal) noise is the noise contribution introduced by the two parasitic resistances r_D and r_S. The magnitude of the current noise is linearly impacted by the junction temperature (in Kelvin). **Equation 13** contains the constants needed for this section, and **Equation 14** contains the equations for the drain and source thermal noise sources. This component is also present and uniform across all frequencies [2].

$$N_{Drain-Thermal}\left(\overline{A^2}\right) = \frac{4k_B T}{r_D}\Delta f \quad N_{Source-Thermal}\left(\overline{A^2}\right) = \frac{4k_B T}{r_S}\Delta f$$

Equation 16, SPICE equations for the Thermal Noise contributions of the Parasitic Resistances.

All the noise current sources occur in parallel to some form of a resistance, as a result, they can be expressed as Thevenin-Norton Equivalent voltage sources. It is critical to note that the Shot and Flicker noise components share a parallel resistance, and as a result can be added together.

So, once the values for all the noise components at any given temperature, drain current, and transconductance have been determined, how can that be converted to Input Referred Voltage Noise? First, here's a sample circuit for computing the noise. Output-Referred Noise is noise occurring at the drain, and Input-Referred Noise is the noise occurring at the gate.

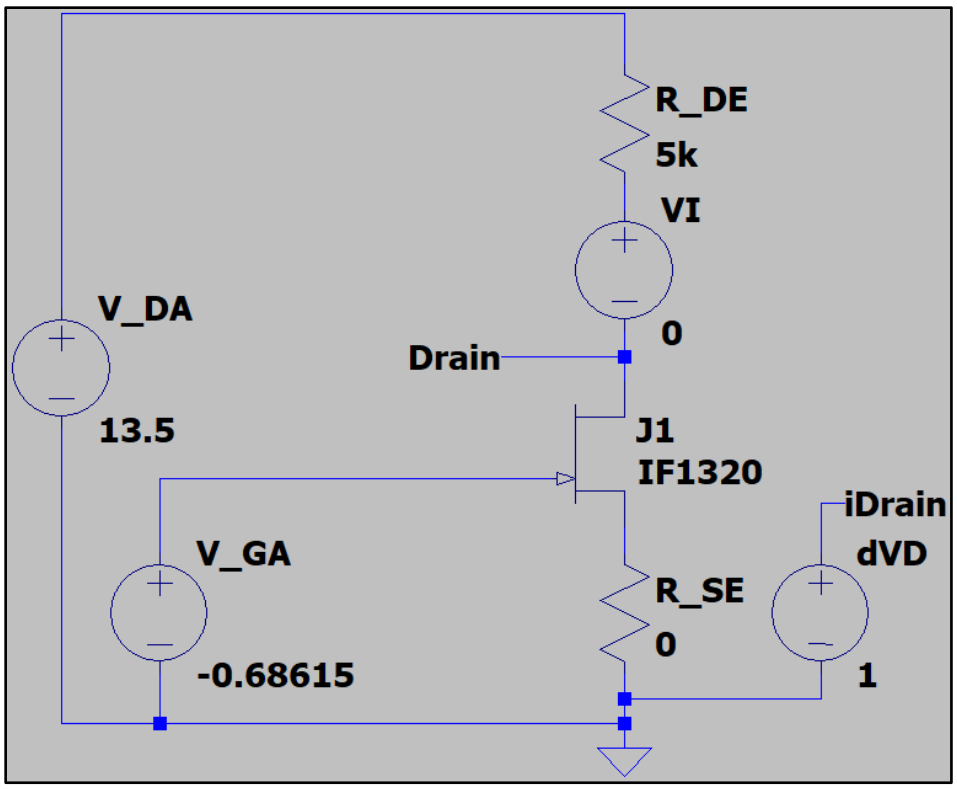

Figure 9, A simple circuit for measuring Voltage or Current Noise in LTSpice. Schematic produced using LTSpice.

To compute the noise at different nodes, we need to convert all the current noise sources into the Output-Referred Current Noise:

$$N_{OR-I}(A) \approx \sqrt{\frac{N_{Drain-Thermal} r_D + N_{Source-Thermal} r_S + (N_{Flicker} + N_{Shot}) R_{DS}}{R_{DS} + r_D + r_S}}$$

Equation 17, Approximate equation for the SPICE Output-Referred Current Noise.

After doing that, we can then calculate the Output or Input-Referred Voltage Noise:

$$N_{OR-V}\left(\frac{V}{\sqrt{Hz}}\right) \approx N_{OR-I} R_{DE} \rightarrow N_{IR-V}\left(\frac{V}{\sqrt{Hz}}\right) \approx \frac{N_{OR-V}}{g_m R_{DE}}$$

Equation 18, Approximate equations for the SPICE Output and Input-Referred Voltage Noise.

To calculate the SPICE parameters needed for accurate noise behavior, you first need to take the measured noise (input-referred) and convert it into output-referred current noise.

$$N_{OR-I}(A) = g_m N_{IR-V}$$

Equation 19, Approximate equations for the SPICE Output and Input-Referred Voltage Noise.

Then since the thermal noises and the shot noise can be calculated, compute those and remove them from the total current noise.

$$N_{Flicker-Calc} = \frac{{N_{OR-I}}^2(R_{DS} + r_D + r_S) - (r_D N_{Thermal-DCalc} + r_S N_{Thermal-SCalc} + R_{DS} N_{Shot-Calc})}{R_{DS}}$$

Equation 20, Approximate equations for the SPICE Output and Input-Referred Voltage Noise.

Then compute the following values (x_V and y_V) and perform a linear regression on them, obtaining the slope (m) and y-intercept (b).

$$x_V = ln(I_D) \qquad y_V = ln(N_{Flicker-Calc}(I_D, f) \cdot f)$$
$$a_F = \text{median}(m) \qquad k_F = \text{median}(e^b)$$

Equation 21, Equations for estimating the AF and KF SPICE parameters.

The results should be somewhat accurate given that the correct I_D, g_m, and T are used for each noise sweep.

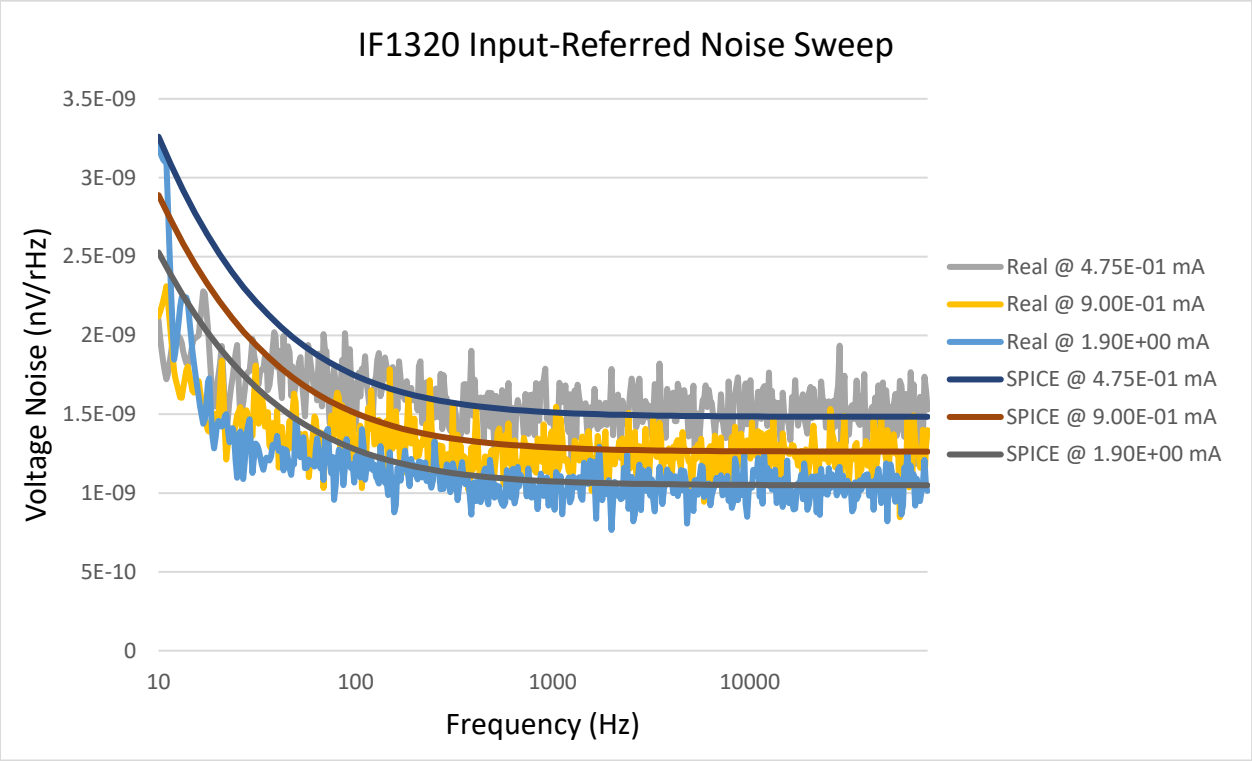

Figure 10, An Input-Referred Voltage Noise Sweep with overlayed SPICE model.

Citations

[1] G. Massobrio and P. Antognetti, Semiconductor Device Modeling with Spice. McGraw-Hill, 2009.

[2] R. Keim, What Is Electrical Noise and Where Does It Come From?. All About Circuits, 2018.