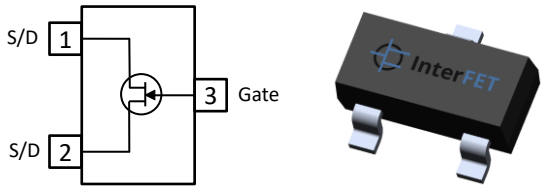
P1086, P1087 P-Channel JFET

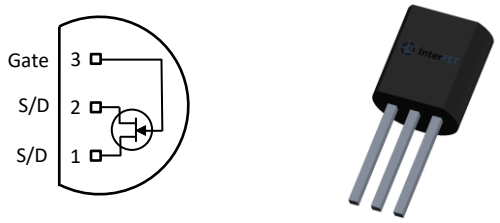
Features

- InterFET P0099F Geometry
- Low noise: 8.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @20V
- Typical $V_{GS(OFF)}$: -2.5V
- Typical I_{DSS}: 12mA
- Typical BV_{GSS}: -35V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- TBD

InterFET Similar Parts

- 2N5116
- U306
- IFN3993

InterFET Dual Parts

- TBD

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The 30V InterFET P1086 and P1087 JFET's are targeted for low noise switching and chopper applications.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
P1086; P1087	Through-Hole	TO-92	Bulk
SMPP1086; SMPP1087	Surface Mount	SOT23	Bulk
SMPP1086TR; SMPP1087TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
P1086COT; P1087COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
P1086CFT; P1087CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		SOT-23	TO-92	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	V
I_{FG}	Continuous Forward Gate Current	50	50	mA
P_D	Continuous Device Power Dissipation[1]	350	500	mW
P	Power Derating[1]	2.8	4	mW/°C
T_J	Operating Junction Temperature	-55 to 150	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

	Parameters	Conditions	P1086 Min	P1086 Max	P1087 Min	P1087 Max	Unit
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 1µA	30		30		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = 15V, V_{DS} = 0V		2		2	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = -1µA		10		5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -20V (Pulsed)	-10		-5		mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = -15V, P1086: V_{GS} = 12V, P1087: V_{GS} = 7V; T_A = 25°C; T_A = 85°C		-10 -0.5		-10 -0.5	nA µA
I_{DGO}	Drain Reverse Current	V_{DG} = -15V, I_S = 0A, T_A = 25°C V_{DG} = -15V, I_S = 0A, T_A = 85°C		2 0.1		2 0.1	nA µA
$V_{DS(ON)}$	Drain to Source ON Voltage	P1086: V_{GS} = 0V, I_D = -6mA P1087: V_{GS} = 0V, I_D = -3mA		-0.5 -0.5		-0.5 -0.5	V
$R_{DS(ON)}$	Static Drain to Source ON Resistance	I_D = -1mA, V_{GS} = 0V		75		150	Ω

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

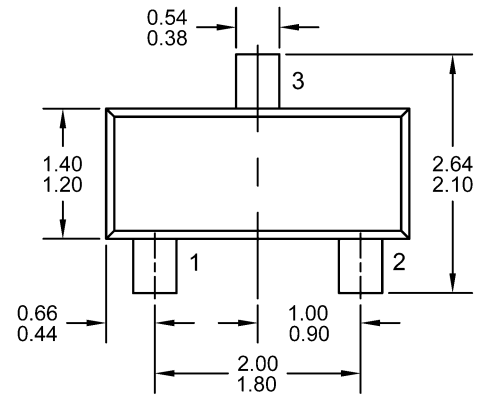
	Parameters	Conditions	P1086 Min	P1086 Max	P1087 Min	P1087 Max	Unit
$R_{DS(ON)}$	Drain to Source ON Resistance	I_D = 0A, V_{GS} = 0V, f = 1kHz		75		150	Ω
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz		45		45	pF
C_{rss}	Reverse Transfer Capacitance	P1086: V_{DS} = 0V, V_{GS} = 12V, f = 1MHz P1087: V_{DS} = 0V, V_{GS} = 7V, f = 1MHz		10 10		10 10	pF
$t_{d(ON)}$	Turn ON Delay Time	V_{DD} = -6V, $V_{GS(ON)}$ = 0V P1086: $V_{GS(OFF)}$ = 12V, $I_{D(ON)}$ = -6mA, R_L = 910Ω P1087: $V_{GS(OFF)}$ = 7V, $I_{D(ON)}$ = -3mA, R_L = 1.8KΩ		15		15	ns
t_r	Rise Time			20		20	ns
$t_{d(OFF)}$	Turn OFF Delay Time			15		25	ns
t_f	Fall Time			50		100	ns

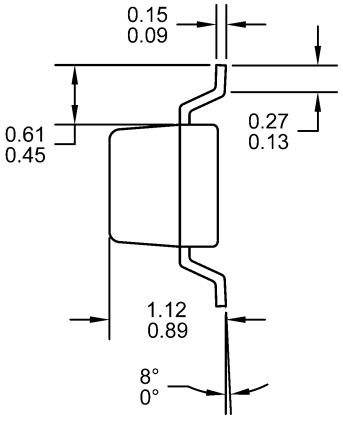
Typical P1086, P1087 Characteristics

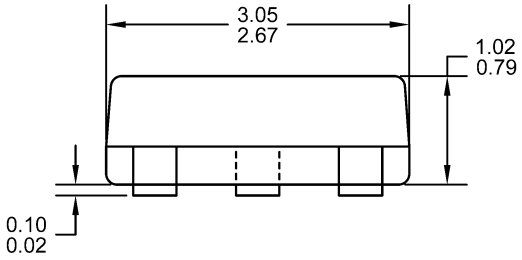
Typical P1086, P1087 Characteristics (Continued)

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

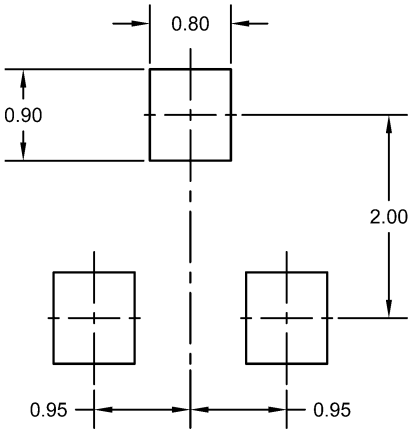






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

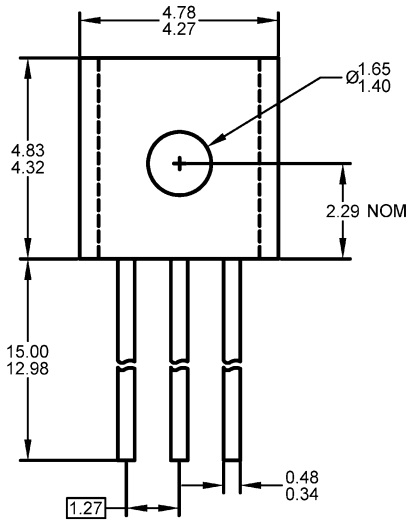
Suggested Pad Layout

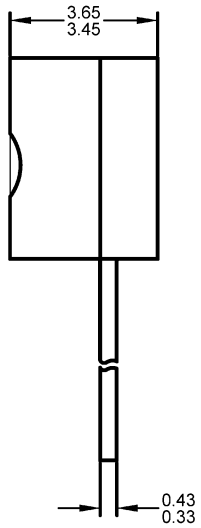


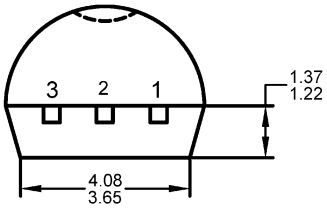
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

TO-92 Mechanical and Layout Data

Package Outline Data

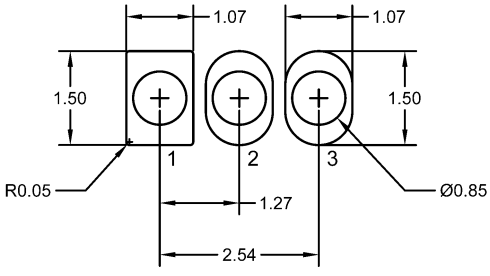






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

Legal Notice

InterFET Corporation reserves the right to make corrections, enhancements, improvements, modifications, and other changes to its semiconductor products without further notice to this document and any product described herein. InterFET does not assume any liability arising out of the application or use of this document or any product described herein. Unless InterFET has explicitly designated an individual product as meeting the requirements of a particular industry standard, InterFET is not responsible for any failure to meet such industry standard requirements.

InterFET Corporation assumes no liability for a customers product design or applications. Corporate designers and others who are developing systems that incorporate InterFET products understand and agree that they remain responsible for using their independent analysis, evaluation and judgment in designing their applications. Corporate designers and others have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications with all applicable regulations, laws and other applicable requirements.

InterFET Corporation resources are provided "as is" with potential faults. InterFET disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any widespread failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights. InterFET shall not be liable for and shall not defend or indemnify designer against any claim, including but not limited to any infringement claim that relates to or is based on any combination of products even if described in InterFET resources or otherwise. In no event shall InterFET be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of InterFET resources or use thereof, and regardless of whether InterFET has been advised of the possibility of such damages.