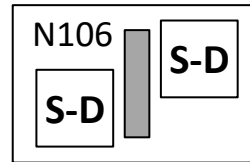


## N106A Process Geometry

### Features

- Cost effective die shrink geometry
- Low gate leakage: 2.0pA @40V typical
- Low Ciss: 3.2pF typical
- Typical BV<sub>GSS</sub>: -50V
- High input impedance
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Small die: 231um X 334um X 203um
- Bond pads: 90um X 90um
- Substrate connected to gate
- Au back-side finish

### Geometry Top View



### Standard Parts

- IFN201A, IFN201, IFN202

### InterFET Similar Geometries

- N0001SH, N0016SH, N0016SS

### InterFET Similar Parts

- 2N4338, 2N4339, 2N4867, 2N4868, 2N4869, J201, J202, 2N3458, 2N3459, 2N3460
- SMP4338, SMP4339, SMP4867, SMP4868, SMP4869, SMPJ201, SMPJ202, SMP3458, SMP3459, SMP3460

### InterFET Similar Dual Parts

- IFN3954-8; IFN5197-9; IFNU231-5; IFNU401-6; IFNU410-2
- SMP3954-8; SMP5197-9; SMPU231-5; SMPU401-6; SMPU410-2

### Applications

- General: amplifiers; Low leakage switches; Signal mixers
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Pre-amplifier speaker drive; Microphone impedance transformation and drive; Phono preamplifiers
- Military/Aero: Radar and communication systems; Missiles and guidance systems; Radiation detection
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment

### Description

The InterFET N106A die is targeted for cost sensitive low noise applications. These parts are ideal for audio mic and preamplifier designs. Gate leakages are typically less than 2pA at room temperatures. Exact crosses for SST201, MMBFJ201, MMBFJ201, J201, and J202 JFETs. Available in waffle pack, matched pair waffle pack, unsawn wafer, and sawn wafer options.

### Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN201COT; IFN201ACOT; IFN202COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN201CFT; IFN201ACFT; IFN202CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



**NOTICE:** Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

## Electrical Characteristics

### Maximum Ratings (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Min	Max	Unit
$V_{RGS}$ Reverse Gate to Source or Drain Voltage	-40		V
$I_{FG}$ Continuous Forward Gate Current		10	mA
$T_J$ Operating Junction Temperature	-55	150	$^\circ\text{C}$
$T_{STG}$ Storage Temperature	-65	175	$^\circ\text{C}$

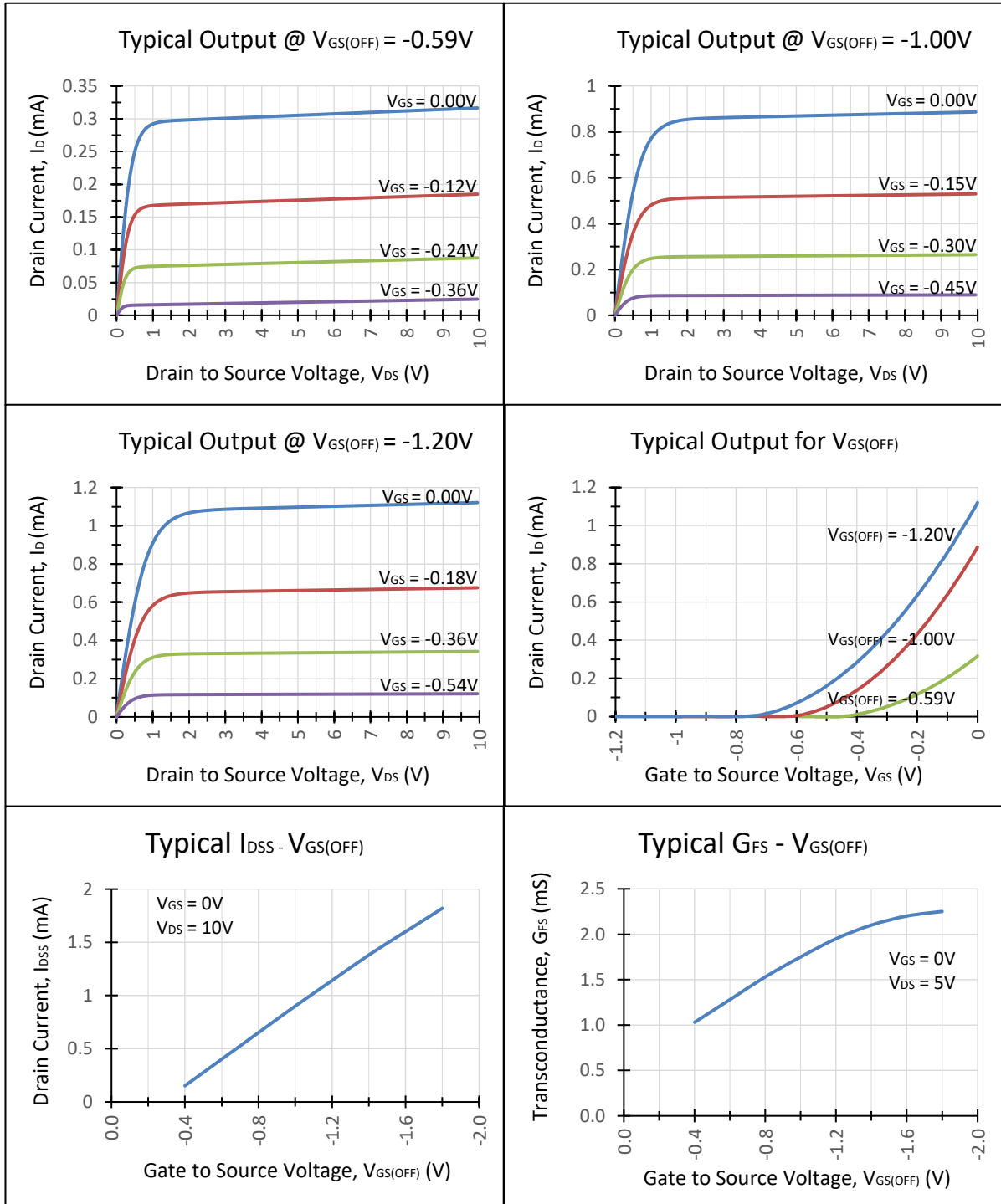
### Static Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	Min	Typ	Max	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	$I_G = -1\mu\text{A}$ , $V_{DS} = 0\text{V}$	-40	-50		V
$I_{GSS}$ Gate to Source Reverse Current	$V_{GS} = -40\text{V}$ , $V_{DS} = 0\text{V}$		-2	-100	pA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10\text{V}$ , $I_D = 1\text{nA}$	-0.4		-2	V
$I_{DSS}$ Drain to Source Saturation Current	$V_{DS} = 10\text{V}$ , $V_{GS} = 0\text{V}$	0.1		2	mA

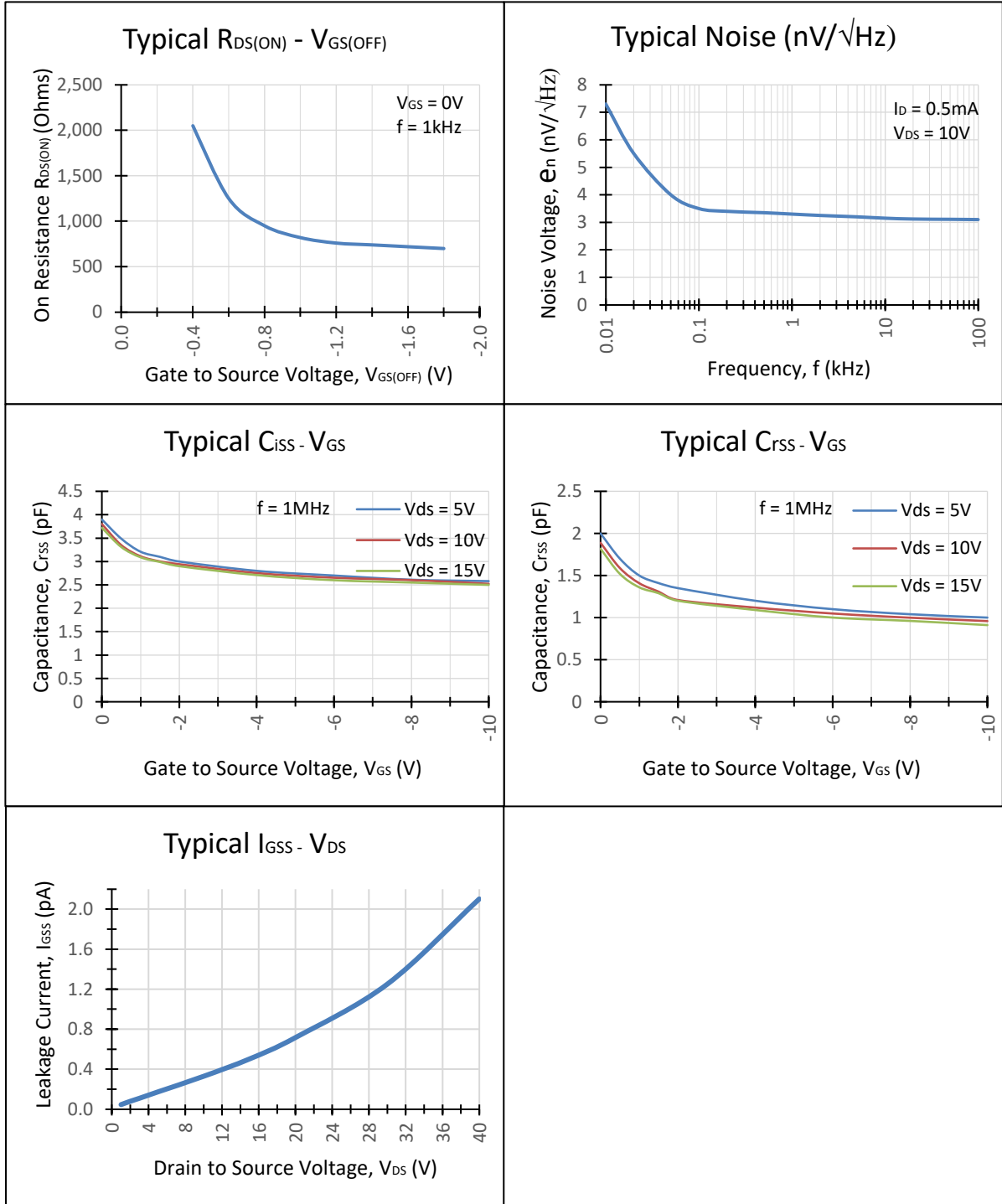
### Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	Min	Typ	Max	Unit
$G_{FS}$ Forward Transconductance	$V_{DS} = 10\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{kHz}$		2		mS
$C_{iss}$ Input Capacitance	$V_{DS} = 10\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$		3.2		pF
$C_{rss}$ Reverse Transfer Capacitance	$V_{DS} = 0\text{V}$ , $V_{GS} = -10\text{V}$ , $f = 1\text{MHz}$		1.5		pF
$e_n$ Noise Voltage	$V_{DS} = 4\text{V}$ , $I_D = 5\text{mA}$ , $f = 1\text{kHz}$		3.0		nV/ $\sqrt{\text{Hz}}$

## Typical Characteristics

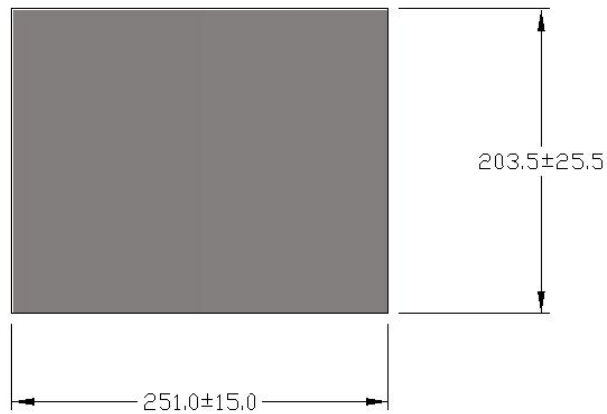
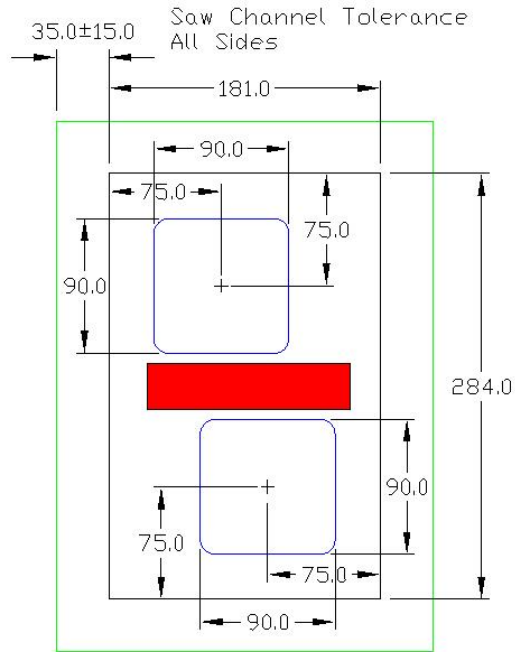


## Typical Characteristics (Continued)



# N106A Die Geometry Mechanical

## Raw Die Dimensions



1. All linear dimensions are in microns (um).

## Compliance and Legal

### Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit [www.InterFET.com/environmental/](http://www.InterFET.com/environmental/).

### Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

### Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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