

J506, J507, J508 Current Regulator Diode

Features

- InterFET [N0016H Geometry](#)
- Low Noise: 5 nV/VHz Typical
- Low Capacitance: 2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

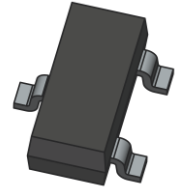
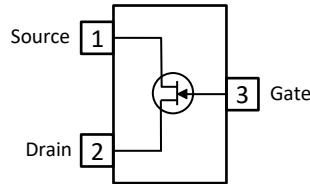
Applications

- Current Regulation
- Current Limiting

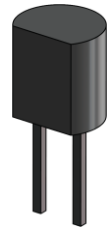
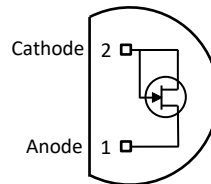
Description

The 50V InterFET J506, J507, and J508 JFET's are targeted for current regulation and limiting applications. The SOT23 package is pinned out as a standard JFET and is required by the user to connect the Gate to the Source or Drain.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		J506 Min	J507 Min	J508 Min	Unit
V _{OP}	Peak Operating Voltage	50	50	50	V
I _{F1}	Forward Current	1.12	1.44	1.9	mA
V _L	Limiting Voltage	1.8 (typ)	2.0 (typ)	2.2 (typ)	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J506; J507; J508	Through-Hole	TO-92-2L	Bulk
SMPJ506; SMPJ507; SMPJ508	Surface Mount	SOT23	Bulk
SMPJ506TR; SMPJ507TR; SMPJ508TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J506COT; J507COT; J508COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J506CFT; J507CFT; J508CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{OP} Peak Operating Voltage	50	V
I_{FG} Continuous Forward Gate Current	20	mA
P_D Continuous Device Power Dissipation	360	mW
P Power Derating	3.27	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 135	$^\circ\text{C}$
T_{STG} Storage Temperature	-55 to 135	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	J506			J507			J508			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{F1} Forward Current	$V_F = 25\text{V}$	1.12	1.4	1.68	1.44	1.8	2.16	1.9	2.4	2.9	mA
V_L Limiting Voltage	$I_F = 0.9 I_{F(\text{MIN})}$		1.8	2.5		2.0	2.8		2.2	3.1	V
V_{OP} Peak Operating Voltage	$I_F = 1.1 I_{F(\text{MAX})}$	50			50			50			V

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	J506			J507			J508			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Z_{fi} Dynamic Impedance	$V_F = 25\text{V}$, $f = 1\text{kHz}$	0.33	1.4		0.2	1.0		0.2	0.7		$\text{M}\Omega$
C_F Anode-Cathode Capacitance	$V_F = 25\text{V}$, $f = 1\text{kHz}$		2			2			2		pF

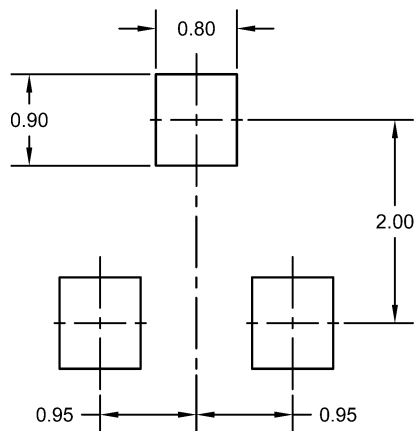
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

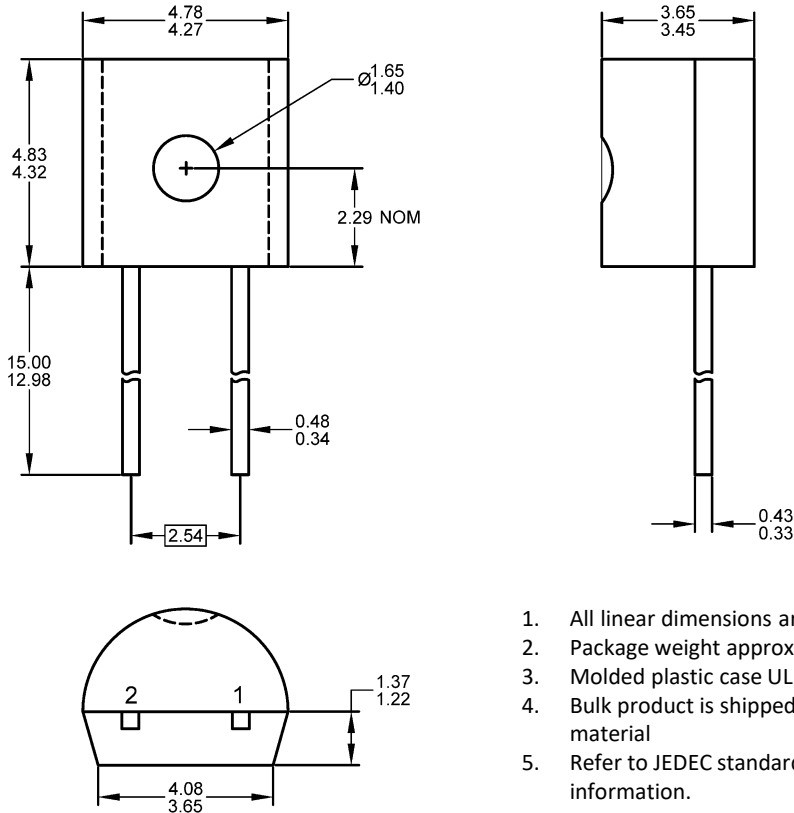
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

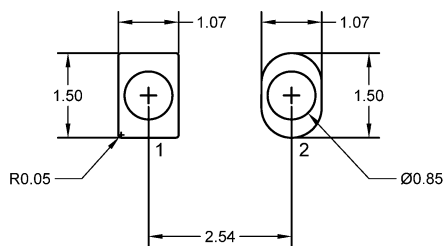
TO-92-2L Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.