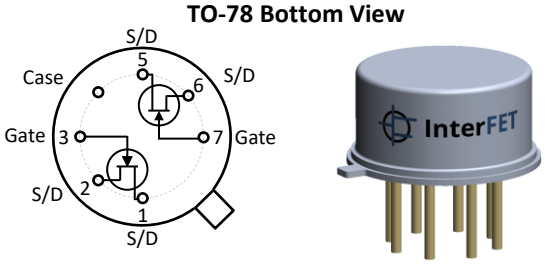
IFNU424, IFNU425, IFNU426 Dual Matched N-Channel JFET

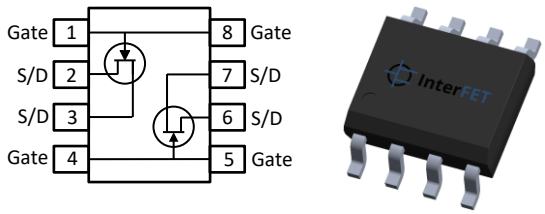
Features

- InterFET N0001H Geometry
- Low gate leakage: 750fA typical @20V
- Low Ciss: 3pF typical
- Typical noise: 2.0 nV/√Hz
- Typical gain: 2mS
- Low cutoff voltage: -1.0 typical
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

TO-78 Bottom View



SOIC8 Top View



NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- TBD

InterFET Similar Parts

- 2N4118-9A

InterFET Dual Parts

- IFNU421-2-3

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -40V InterFET IFNU424, IFNU425, and IFNU426 JFET's are targeted for ultra high input impedance applications for differential amplification and impedance matching. Gate leakages are less than 1pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU424; IFNU425; IFNU426	Through-Hole	TO-78	Bulk
SMPU424; SMPU425; SMPU426;	Surface Mount	SOIC8	Bulk
SMPU424TR; SMPU425TR; SMPU426TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU424COT; IFNU425COT; IFNU426COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU424CFT; IFNU425CFT; IFNU426CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-71	SOIC-8	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	V
I_{FG}	Continuous Forward Gate Current	50	50	mA
P_D	Continuous Device Power Dissipation[1]	500	350	mW
P	Power Derating[1]	3.3	2.8	mW/°C
T_J	Operating Junction Temperature	-65 to 175	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	INFU424, INFU425, INFU426			Unit
			Min	Typ	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA,V_{DS} = 0V	-40	-60		V
BV_{G1G2}	Gate to Gate Breakdown Voltage	I_G = -1µA, I_D = 0A, I_S = 0A	±40			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V, T_A = 25°C V_{GS} = -20V, V_{DS} = 0V, T_A = 125°C			-3 -3	pA nA
I_G	Gate Operating Current	V_{DS} = 10V, I_D = 30µA, T_A = 25°C V_{DS} = 10V, I_D = 30µA, T_A = 125°C			-0.5 -500	pA pA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA	-0.4		-3	V
V_{GS}	Gate Source Voltage	V_{DS} = 10V, I_D = 30µA			-2.9	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	60	1800		µA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

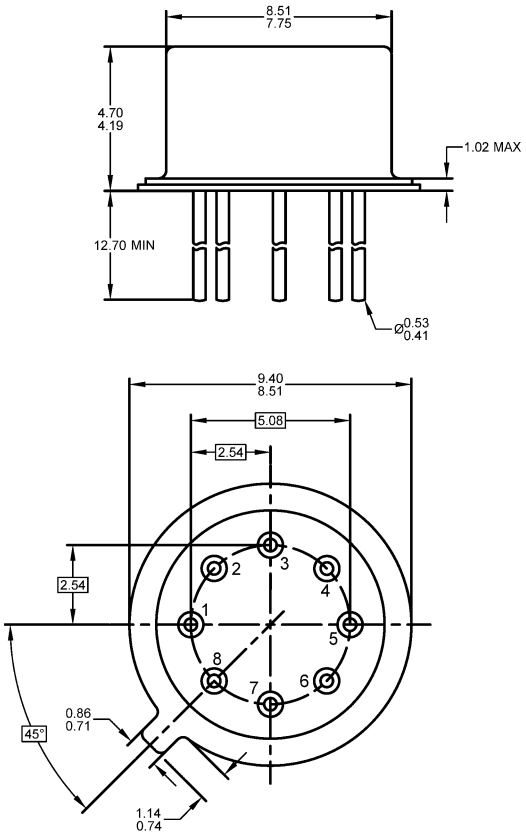
Parameters		Conditions		INFU424, INFU425, INFU426			Unit
				Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz		100		1500	µS
G_{OS}	Output Conductance	V_{DS} = 10V, I_D = 30µA, f = 1kHz				3	µS
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz				3	pF
C_{rss}	Reverse Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz				1.5	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 30µA, f = 10Hz			20	70	nV/√Hz
NF	Noise Figure	V_{DS} = 10V, I_D = 30µA, f = 10Hz, R_G = 1MΩ				1	dB
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 30µA	INFU424 INFU425 INFU426			10 15 25	mV
$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate Source Voltage with Temperature	V_{DS} = 10V, I_D = 30µA T_A = -55°C, T_B = 25°C, T_C = 125°C	INFU424 INFU425 INFU426			1 2.5 5	mV/°C
CMRR	Common Mode Rejection Ratio	V_{DD} = 10V to 20V, I_D = 30µA	INFU424 INFU425 INFU426	90 80 80			dB

Typical IFNU424, IFNU425, IFNU426 Characteristics

Typical IFNU424, IFNU425, IFNU426 Characteristics (Continued)

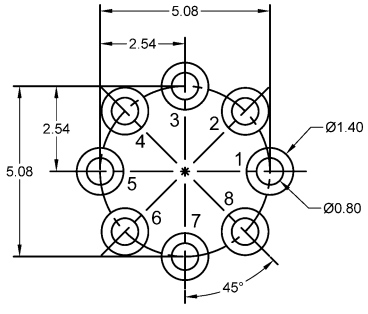
TO-78 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

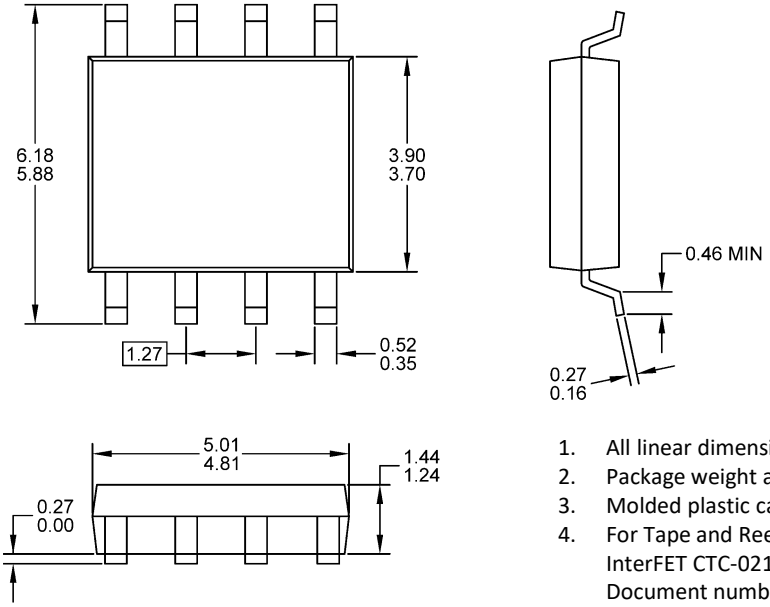
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

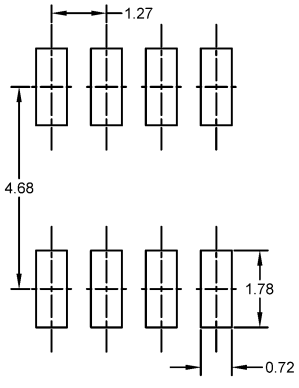
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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