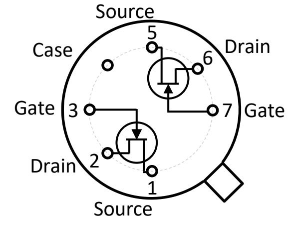
IFNU421, IFNU422, IFNU423 Dual Matched N-Channel JFET

Features

- InterFET N0001H Geometry
- Low Leakage: 0.25 pA Typical
- Low Input Capacitance: 2.0 pF Typical
- High Input Impedance
- Replacement for U421, U422, U423
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

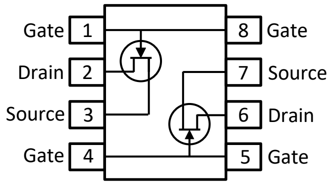
TO-78 Bottom View



Applications

- Low Leakage Input Buffer
- High Frequency Amplifier/Buffer
- Ultrahigh Impedance Pre-Amplifier
- Impedance Converters

SOIC8 Top View



Description

The -40V InterFET IFNU421, IFNU422, and IFNU423 JFET's are targeted for ultra high input impedance applications for differential amplification and impedance matching. Gate leakages are less than 1pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters		IFNU421 Min	IFNU422 Min	IFNU423 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	60	60	60	µA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.4	-0.4	-0.4	V
G_{FS}	Forward Transconductance	100	100	100	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU421; IFNU422; IFNU423	Through-Hole	TO-78	Bulk
SMPU421; SMPU422; SMPU423;	Surface Mount	SOIC8	Bulk
SMPU421TR; SMPU422TR; SMPU423TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU421COT; IFNU422COT; IFNU423COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU421CFT; IFNU422CFT; IFNU423CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	400	mW
P	Power Derating	3.2	mW/°C
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

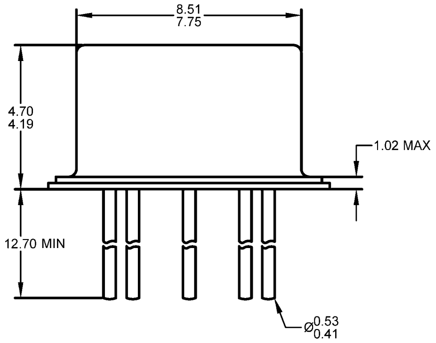
Parameters		Conditions	IFNU421, IFNU422, IFNU423			Unit
			Min	Typ	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-40	-60		V
BV_{G1G2}	Gate to Gate Breakdown Voltage	I_G = -1µA, I_D = 0A, I_S = 0A	±40			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V, T_A = 25°C V_{GS} = -20V, V_{DS} = 0V, T_A = 125°C			-1 -1	pA nA
I_G	Gate Operating Current	V_{DS} = 10V, I_D = 30µA, T_A = 25°C V_{DS} = 10V, I_D = 30µA, T_A = 125°C			-0.25 -250	pA pA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA	-0.4		-2	V
V_{GS}	Gate Source Voltage	V_{DS} = 10V, I_D = 30µA			-1.8	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	60		1000	µA

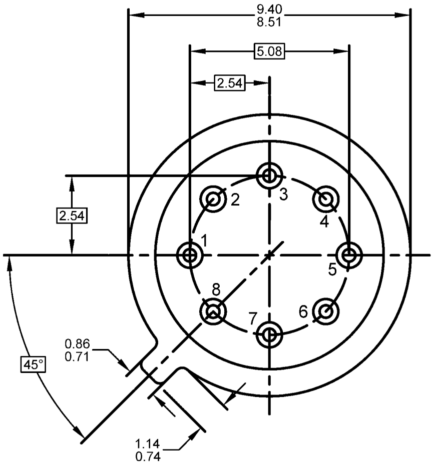
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IFNU421, IFNU422, IFNU423			Unit
			Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz	100		1500	µS
G_{OS}	Output Conductance	V_{DS} = 10V, I_D = 30µA, f = 1kHz			3	µS
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz			3	pF
C_{rss}	Reverse Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz			1.5	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 30µA, f = 10Hz		20	70	nV/√Hz
NF	Noise Figure	V_{DS} = 10V, I_D = 30µA, f = 10Hz, R_G = 10MΩ			1	dB
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 30µA — IFNU421 IFNU422 IFNU423			10 15 25	mV
$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate Source Voltage with Temperature	V_{DS} = 10V, I_D = 30µA, T_A = -55°C, T_B = 25°C, T_C = 125°C — IFNU421 IFNU422 IFNU423			1 2.5 5	mV/°C
CMRR	Common Mode Rejection Ratio	V_{DD} = 10V to 20V, I_D = 30µA — IFNU421 IFNU422 IFNU423	90 80 80			dB

TO-78 Mechanical and Layout Data

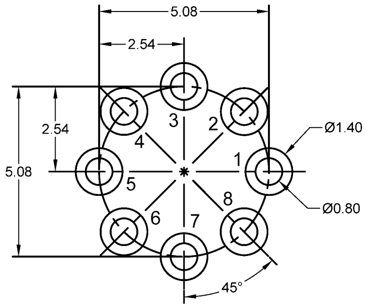
Package Outline Data





1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

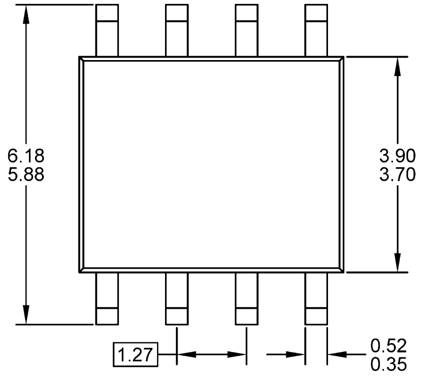
Suggested Through-Hole Layout

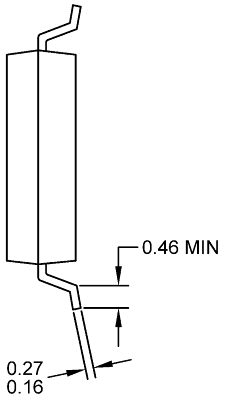


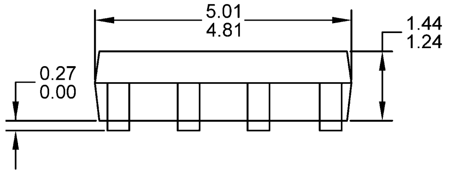
1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

SOIC8 Mechanical and Layout Data

Package Outline Data

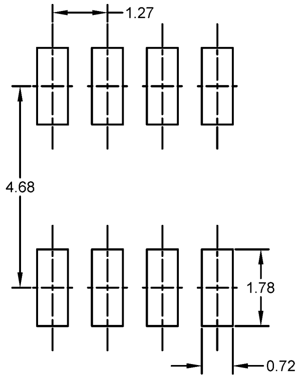






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.