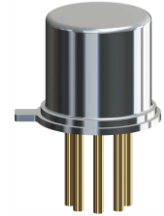
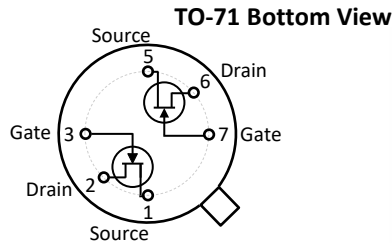


IFNU404, IFNU405, IFNU406 Dual Matched N-Channel JFET

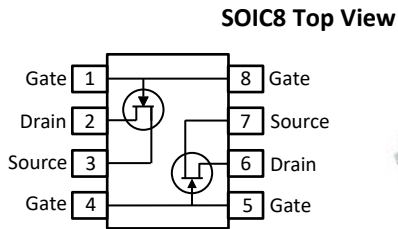
Features

- InterFET [N0016H Geometry](#)
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 3.5 pF Typical
- High Input Impedance
- Replacement for U404,5,6
- RoHS Compliant
- SMT, TH, and Bare Die Package options.



Applications

- Low Noise Differential Amplifier
- Differential Amplifier
- JFET Input Op-Amps



Description

The -50V InterFET IFNU404, IFNU405, and IFNU406 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters	IFNU404 Min	IFNU405 Min	IFNU406 Min	Unit
BV _{GSS} Gate to Source Breakdown Voltage	-50	-50	-50	V
I _{DSS} Drain to Source Saturation Current	0.5	0.5	0.5	mA
V _{GS(off)} Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
G _{FS} Forward Transconductance	2	2	2	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU404; IFNU405; IFNU406	Through-Hole	TO-71	Bulk
SMPU404; SMPU405; SMPU406	Surface Mount	SOIC8	Bulk
SMPU404; SMPU405; SMPU406	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU404COT; IFNU405COT; IFNU406COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU404CFT; IFNU405CFT; IFNU406CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V _{RGS} Reverse Gate Source and Gate Drain Voltage	-50	V
I _{FG} Continuous Forward Gate Current	50	mA
P _D Continuous Device Power Dissipation	300	mW
P Power Derating	2.8	mW/°C
T _J Operating Junction Temperature	-55 to 125	°C
T _{STG} Storage Temperature	-65 to 150	°C

Static Characteristics (@ T_A = 25°C, Unless otherwise specified)

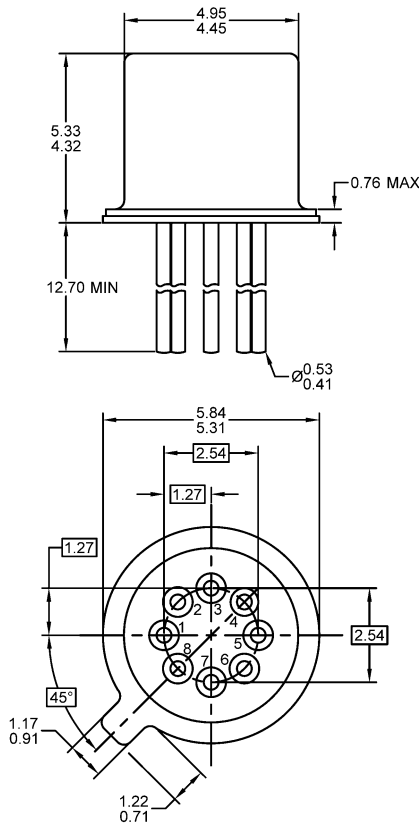
Parameters	Conditions	IFNU404, IFNU405, IFNU406			Unit
		Min	Typ	Max	
V _{(BR)GSS} Gate to Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0V	-50			V
I _{GSS} Gate to Source Reverse Current	V _{GS} = -30V, V _{DS} = 0V			-25	pA
I _G Gate Operating Current	V _{DS} = 15V, I _D = 200μA, T _A = 125 °C V _{DS} = 15V, I _D = 200μA, T _A = 125 °C			-15 -10	pA nA
V _{GS(OFF)} Gate to Source Cutoff Voltage	V _{DS} = 20V, I _D = 1nA	-0.5		-2.5	V
V _{GS} Gate Source Voltage	V _{DS} = 20V, I _D = 200μA	-0.2		-2.3	V
I _{DSS} Drain to Source Saturation Current	V _{DS} = 20V, V _{GS} = 0V (Pulsed)	0.5		10	mA

Dynamic Characteristics (@ T_A = 25°C, Unless otherwise specified)

Parameters	Conditions	IFNU404, IFNU405, IFNU406			Unit
		Min	Typ	Max	
G _{FS} Forward Transconductance	V _{DS} = 10V, V _{GS} = 0V, f = 1kHz V _{DS} = 15V, I _D = 200μA, f = 1kHz	2 1		7 2	mS
G _{OS} Output Conductance	V _{DS} = 10V, V _{GS} = 0V, f = 1kHz V _{DS} = 15V, I _D = 200μA, f = 1kHz			20 2	μS
C _{ISS} Input Capacitance	V _{DS} = 15V, I _D = 200μA, f = 1MHz			8	pF
C _{RSS} Reverse Capacitance	V _{DS} = 15V, I _D = 200μA, f = 1MHz			3	pF
e _n Equivalent Circuit Input Noise Voltage	V _{DS} = 20V, I _D = 200μA, f = 100Hz			20	nV/√Hz
V _{GS1} - V _{GS2} Differential Gate Source Voltage	V _{DS} = 10V, I _D = -200μA			15 20 40	mV
$\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature	V _{DS} = 10V, I _D = 200μA T _A = 25°C, T _B = 85°C			4 5 5	mV/°C
CMRR Common Mode Rejection Ratio	V _{DD} = 10V to 20V, I _D = 200μA		95 90 90		dB

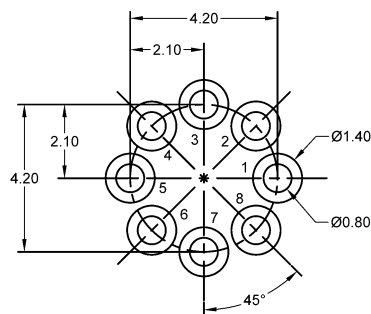
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

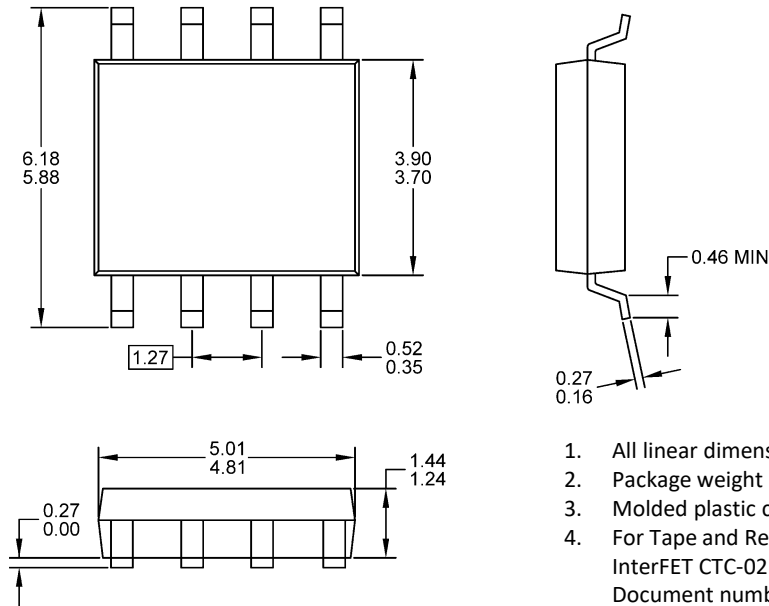
Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

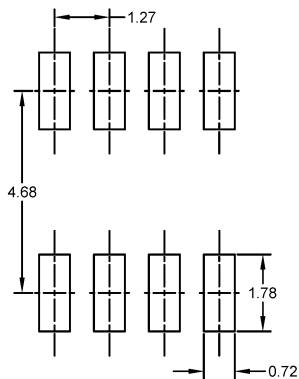
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.