

# IFNU257 Dual Matched N-Channel JFET

## Features

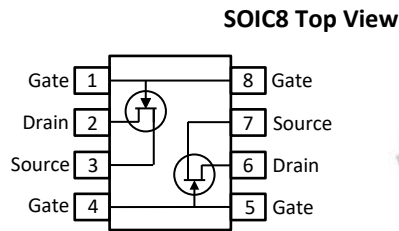
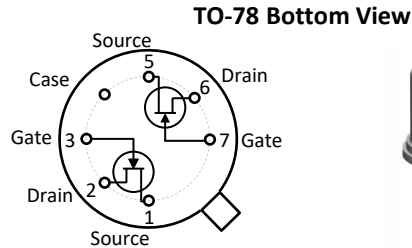
- InterFET [N0030L Geometry](#)
- Low Leakage: 4.0pA Typical
- Low Input Capacitance: 5.0pF Typical
- Replacement for U257
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

## Applications

- Wideband Differential Amplifiers
- Audio Amplifiers

## Description

The -25V InterFET IFNU257 JFET is targeted for wideband differential amplifier applications. Gate leakages are typically less than 4pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



## Product Summary

Parameters	IFNU235 Min	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	-25	V
$I_{DSS}$ Drain to Source Saturation Current	5	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-1	V
$G_{FS}$ Forward Transconductance	4.5	mS

## Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU257	Through-Hole	TO-78	Bulk
SMPU257	Surface Mount	SOIC8	Bulk
SMPU257TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU257COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU257CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

\* Bare die packaged options are designed for matched specifications but not 100% tested



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Value	Unit
$V_{RGS}$ Reverse Gate Source and Gate Drain Voltage	-25	V
$I_{FG}$ Continuous Forward Gate Current	50	mA
$P_D$ Continuous Device Power Dissipation	300	mW
$P$ Power Derating	4	mW/ $^\circ\text{C}$
$T_J$ Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
$T_{STG}$ Storage Temperature	-65 to 150	$^\circ\text{C}$

### Static Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

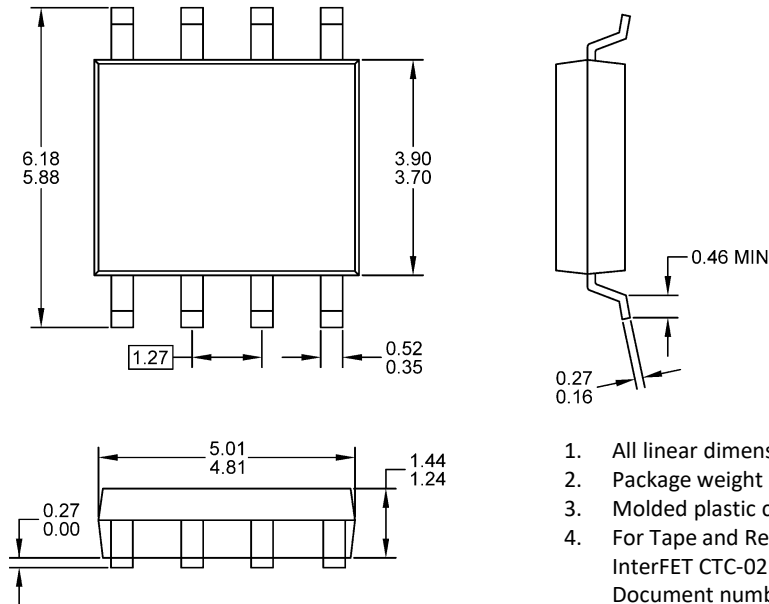
Parameters	Conditions	IFNU257		Unit
		Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-25		V
$I_{GSS}$ Gate to Source Reverse Current	$V_{GS} = -15V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -15V, V_{DS} = 0V, T_A = 150^\circ\text{C}$		-100 -250	pA nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1\text{nA}$	-1	-5	V
$I_{DSS}$ Drain to Source Saturation Current	$V_{DS} = 10V, V_{GS} = 0V$ (Pulsed)	5	40	mA

### Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	IFNU257		Unit
		Min	Max	
$G_{FS}$ Forward Transconductance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{kHz}$ $V_{DS} = 10V, I_D = 5\text{mA}, f = 100\text{MHz}$	4.5 4.5	10 10	mS
$G_{OS}$ Output Conductance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{kHz}$ $V_{DS} = 10V, I_D = 5\text{mA}, f = 100\text{MHz}$		200 200	$\mu\text{S}$
$C_{iss}$ Input Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		5	pF
$C_{rss}$ Reverse Transfer Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		1.2	pF
$e_n$ Equivalent Circuit Input Noise Voltage	$V_{DS} = 10V, I_D = 5\text{mA}, f = 10\text{kHz}$		30	nV/ $\sqrt{\text{Hz}}$
$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage	$V_{DS} = 10V, I_D = 5\text{mA}$		100	mV
$ G_{OS1} - G_{OS2} $ Differential Output Conductance	$V_{DS} = 10V, I_D = 5\text{mA}$		20	$\mu\text{S}$
$I_{DSS1}$ $I_{DSS2}$ Co-saturation Drain Current Ratio	$V_{DS} = 10V, V_{GS} = 0V$	0.85	1	-

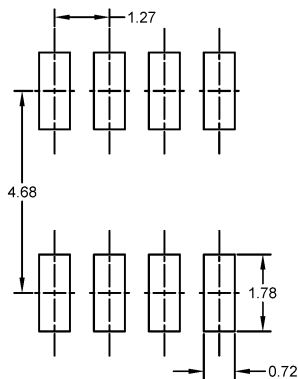
## SOIC8 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

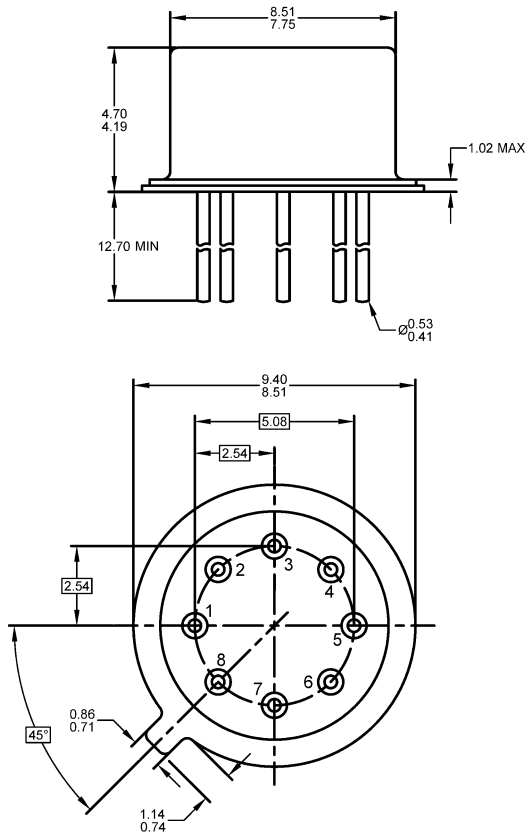
### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

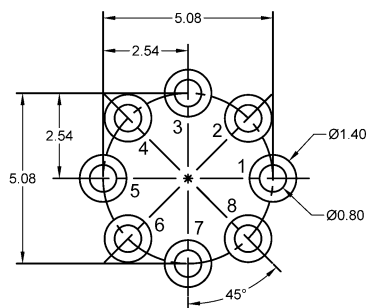
## TO-78 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 7.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.