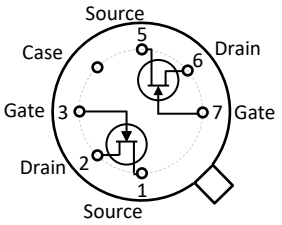
IFN5911, IFN5912 Dual Matched N-Channel JFET

Features

- InterFET N0030L Geometry
- Low Noise: 4.0 nV/√Hz Typical
- Low Leakage: 10pA Typical
- Low Input Capacitance: 5.0 pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

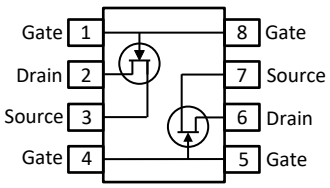
TO-78 Bottom View



Applications

- VHF Amplifiers
- Wideband Differential Amplifiers

SOIC8 Top View



Description

The -25V InterFET IFN5911 and IFN 5912 JFET's are targeted for wideband differential amplifiers. Gate leakages are less than 10pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters		IFN5911 Min	IFN5912 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-25	-25	V
I_{DSS}	Drain to Source Saturation Current	7	7	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	-1	V
G_{FS}	Forward Transconductance	3000	3000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN5911; IFN5912	Through-Hole	TO-78	Bulk
SMP5911; SMP5912	Surface Mount	SOIC8	Bulk
SMP5911; SMP5912	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN5911COT; IFN5912COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFN5911CFT; IFN5912CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-50	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	250	mW
P	Power Derating	4.3	mW/°C
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

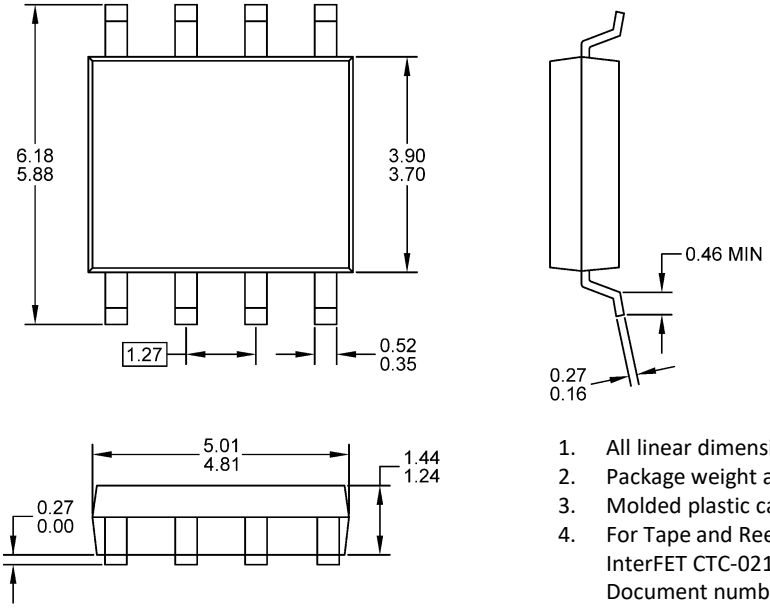
Parameters		Conditions	IFN5911		IFN5912		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-25		-25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -15V, V_{DS} = 0V, T_A = 25°C V_{GS} = -15V, V_{DS} = 0V, T_A = 150°C		-100 -250		-100 -250	pA nA
I_G	Gate Operating Current	V_{DG} = 10V, I_D = 5mA, T_A = 25°C V_{DG} = 10V, I_D = 5mA, T_A = 125°C		-100 -100		-100 -100	pA nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA	-1	-5	-1	-5	V
V_{GS}	Gate Source Voltage	V_{DS} = 10V, I_D = 5mA	-0.3	-4	-0.3	-4	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	7	40	7	40	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IFN5911		IFN5912		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 5mA, f = 1kHz V_{DS} = 10V, I_D = 5mA, f = 100MHz	3000 3000	10000 10000	3000 3000	10000 10000	µS
G_{OS}	Output Conductance	V_{DS} = 10V, I_D = 5mA, f = 1kHz V_{DS} = 10V, I_D = 5mA, f = 100MHz		100 150		100 150	µS
C_{iss}	Input Capacitance	V_{DS} = 10V, I_D = 5mA, f = 1MHz		5		5	pF
C_{rss}	Reverse Capacitance	V_{DS} = 10V, I_D = 5mA, f = 1MHz		1.2		1.2	pF
NF	Noise Figure	V_{DS} = 10V, I_D = 5mA, f = 10Hz, R_G = 100KΩ		1		1	dB
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 5mA, f = 10kHz		20		20	nV/√Hz
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DS} = 10V, I_D = 5mA, T_A = 125°C		20		20	nA
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio	V_{DS} = 10V, V_{GS} = 0V	0.95	1	0.95	1	-
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 5mA		10		15	mV
$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate Source Voltage with Temperature	V_{DS} = 10V, I_D = 5mA, T_A = -55°C, T_B = 25°C T_A = 25°C, T_B = 125°C		2.5 2		5 4	mV/°C
g_{fs1}/g_{fs2}	Transconductance Ratio	V_{DS} = 10V, I_D = 5mA	0.95	1	0.95	1	-

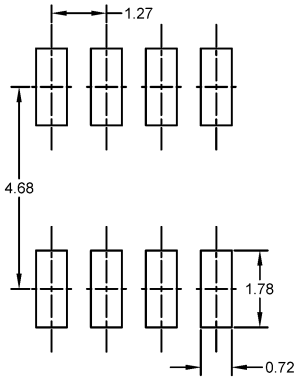
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

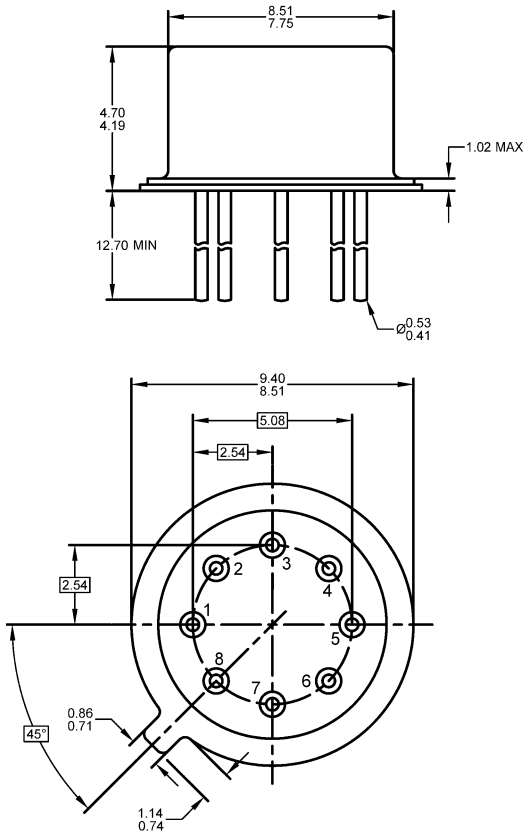
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

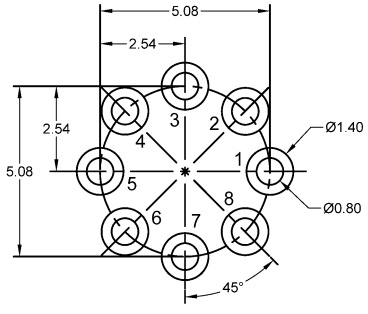
TO-78 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 7.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.