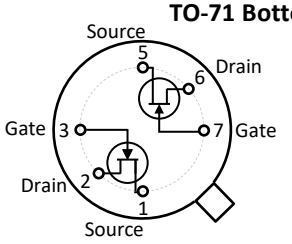
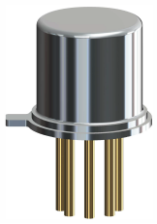
IFN5564, IFN5565, IFN5566 Dual Matched N-Channel JFET

Features

- InterFET N0072S Geometry
- Low Noise: 2.5 nV/√Hz Typical
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 6.5 pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

TO-71 Bottom View

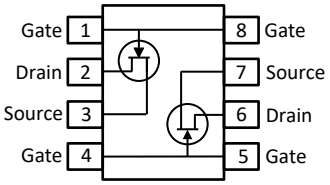




Applications

- Wide Band Differential Amplifier
- Commutators

SOIC8 Top View



Description

The -40V InterFET IFN5564, IFN5565, and IFN5566 JFET's are targeted for wide bandwith differential amplifiers and commutators. Gate leakages are less than 10pA at room temperatures. The IFN5564 is matched down to 5mV. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters		IFN5564 Min	IFN5565 Min	IFN5566 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	5	5	5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
G_{FS}	Forward Transconductance	7000	7000	7000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN5564; IFN5565; IFN5566	Through-Hole	TO-71	Bulk
SMP5564; SMP5565; SMP5566	Through-Hole	SOIC8	Bulk
SMP5564TR; SMP5565TR; SMP5566TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN5564COT; IFN5565COT; IFN5566COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFN5564CFT; IFN5565CFT; IFN5566CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	650	mW
P	Power Derating	3.3	mW/°C
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

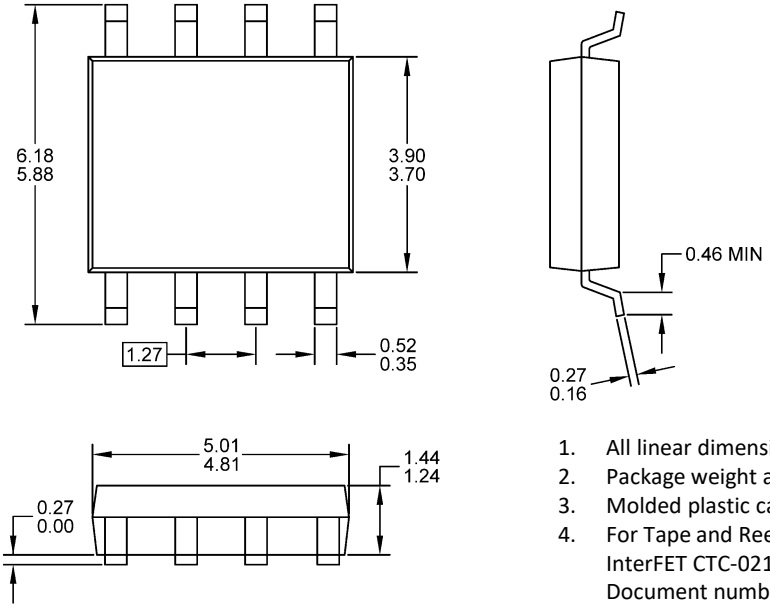
Parameters		Conditions	IFN5564, IFN5565, IFN5566 Min	IFN5564, IFN5565, IFN5566 Max	Unit
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V, T_A = 25°C V_{GS} = -20V, V_{DS} = 0V, T_A = 150°C		-100 -200	pA nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 1nA	-0.5	-3	V
$V_{GS(F)}$	Gate Source Forward Voltage	V_{DS} = 0V, I_G = 2mA		1	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 15V, V_{GS} = 0V (Pulsed)	5	30	mA
$R_{DS(ON)}$	Static Drain to Source ON Resistance	V_{GS} = 0V, I_D = 1mA		100	Ω

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions		IFN5564, IFN5565, IFN5566 Min	IFN5564, IFN5565, IFN5566 Max	Unit
G_{FS}	Forward Transconductance	V_{DS} = 15V, I_D = 2mA, f = 1kHz V_{DS} = 15V, I_D = 2mA, f = 100MHz		7000 7000	12500	µhmo
G_{OS}	Output Conductance	V_{DS} = 15V, I_D = 2mA f = 1kHz			45	µhmo
C_{iss}	Input Capacitance	V_{DS} = 15V, I_D = 2mA, f = 1MHz			12	pF
C_{rss}	Reverse Capacitance	V_{DS} = 15V, I_D = 2mA, f = 1MHz			3	pF
NF	Noise Figure	V_{DS} = 15V, I_D = 2mA, f = 10Hz, R_G = 1MΩ			1	dB
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 15V, I_D = 2mA, f = 10Hz			50	nV/√Hz
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio	V_{DS} = 15V, V_{GS} = 0V (Pulsed)		0.95	1	-
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 15V, I_D = 2mA	IFN5564 IFN5565 IFN5566		5 10 20	mV
$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate Source Voltage with Temperature	V_{DS} = 15V, I_D = 2mA T_A = 25°C to -55°C [0.8,2,4] T_A = 25°C to 125°C [1,2.5,5]	IFN5564 IFN5565 IFN5566		0.8 1 2 2.5 4 5	mV/°C
g_{fs1}/g_{fs2}	Transconductance Ratio	V_{DS} = 15V, I_D = 2mA	IFN5564 IFN5565 IFN5566	0.95 0.9 0.9	1 1 1	-

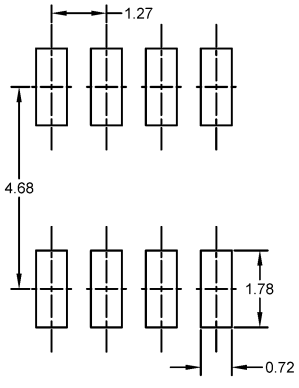
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

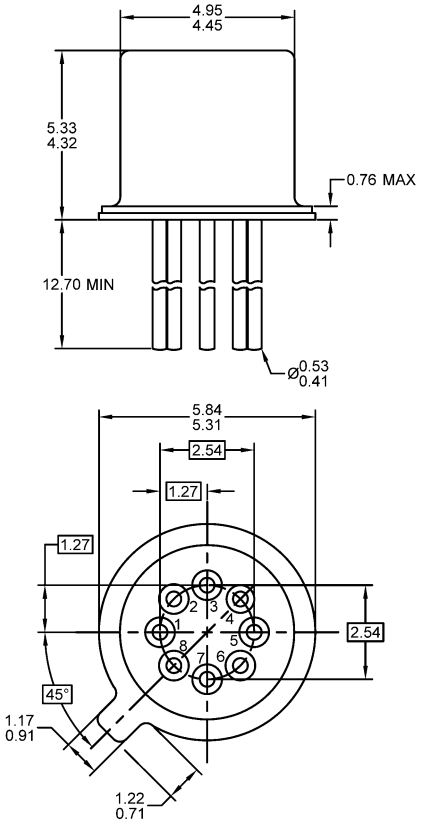
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

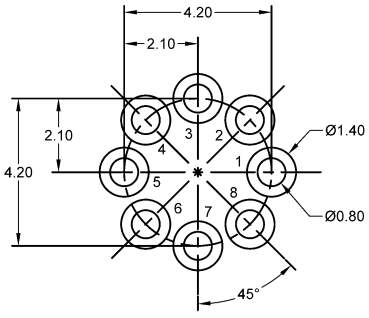
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.