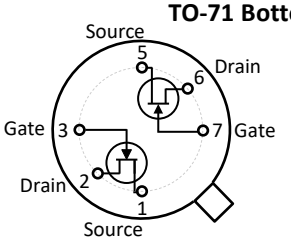
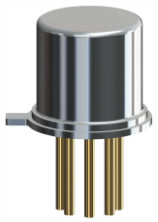
IFN5197, IFN5198, IFN5199 Dual Matched N-Channel JFET

Features

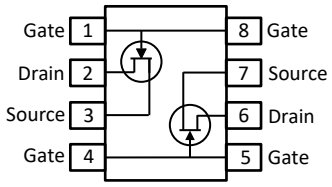
- InterFET N0016H Geometry
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 3.5 pF Typical
- High Input Impedance
- Replacement for IFN5197,8,9
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

TO-71 Bottom View





SOIC8 Top View



Applications

- Low Noise Differential Amplifier
- Differential Amplifier
- JFET Input Op-Amps

Description

The -50V InterFET IFN5197, IFN5198, and IFN5199 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters		IFN5197 Min	IFN5198 Min	IFN5199 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-50	-50	-50	V
I_{DSS}	Drain to Source Saturation Current	0.7	0.7	0.7	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.7	-0.7	-0.7	V
G_{FS}	Forward Transconductance	0.7	0.7	0.7	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN5197; IFN5198; IFN5199	Through-Hole	TO-71	Bulk
SMP5197; SMP5198; SMP5199	Surface Mount	SOIC8	Bulk
SMP5197; SMP5198; SMP5199	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN5197COT; IFN5198COT; IFN5199COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFN5197CFT; IFN5198CFT; IFN5199CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-50	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	250	mW
P	Power Derating	4.3	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

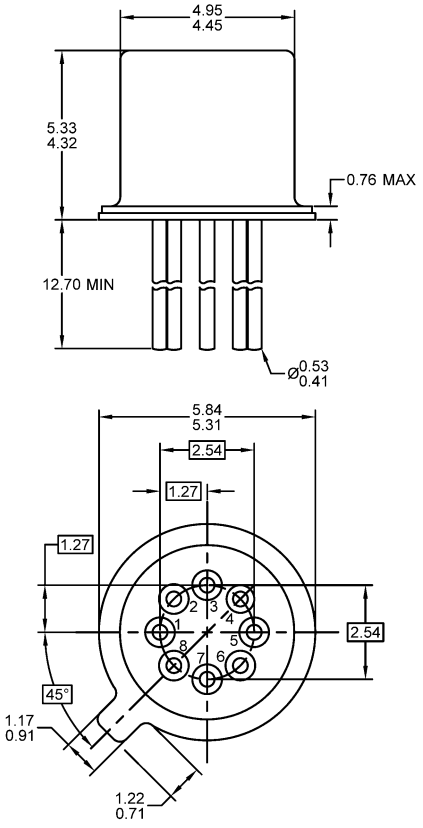
Parameters		Conditions	IFN5197, IFN5198, IFN5199			Unit
			Min	Typ	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-50			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -30V, V_{DS} = 0V, T_A = 25°C V_{GS} = -30V, V_{DS} = 0V, T_A = 150°C			-25 -50	pA nA
I_G	Gate Operating Current	V_{DS} = 20V, I_D = 200µA, T_A = 25°C V_{DS} = 20V, I_D = 200µA, T_A = 125°C			-15 -15	pA nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-0.7		-4.0	V
V_{GS}	Gate Source Voltage	V_{DS} = 20V, I_D = 200µA	-0.2		-3.8	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 20V, V_{GS} = 0V (Pulsed)	0.7		7	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions		IFN5197, IFN5198, IFN5199			Unit
				Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz V_{DS} = 20V, I_D = 200µA, f = 1kHz		1 0.7		4 1.6	mS
G_{OS}	Output Conductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz V_{DS} = 20V, I_D = 200µA, f = 1kHz				50 4	µS
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz				6	pF
C_{rss}	Reverse Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz				2	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 20V, I_D = 200µA, f = 1kHz				20	nV/√Hz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 20V, I_D = -200µA	IFN5197 IFN5198 IFN5199			5 10 15	mV
$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate Source Voltage with Temperature	V_{DS} = 20V, I_D = 200µA T_A = 25°C, T_B = 125°C	IFN5197 IFN5198 IFN5199			1 2.5 4	mV/°C

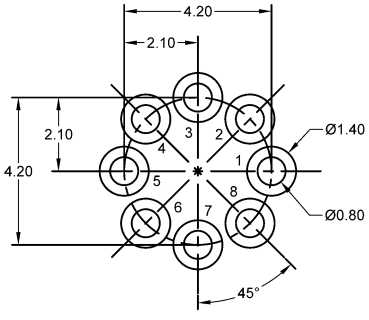
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

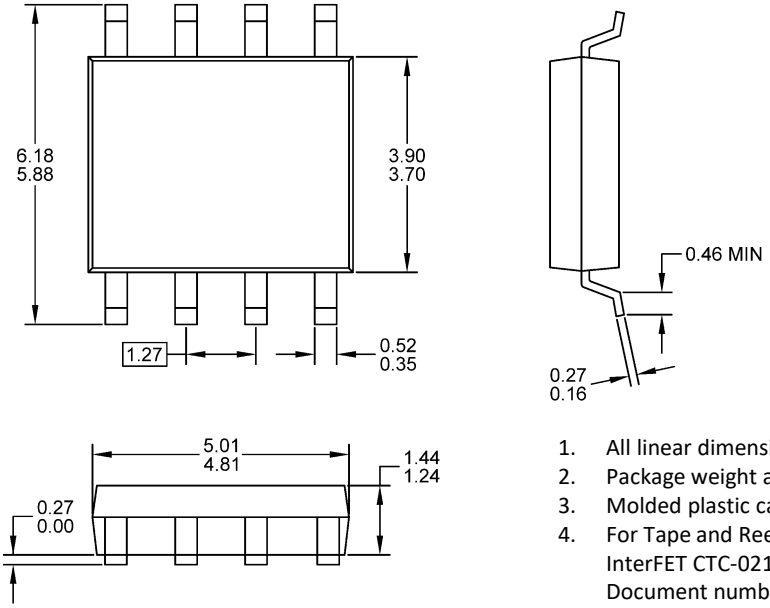
Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

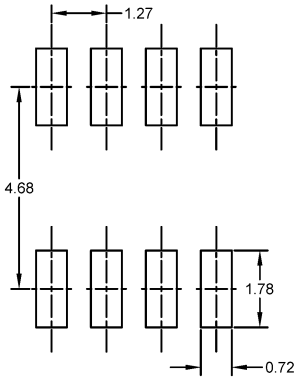
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.