

IFN3993/A, IFN3994/A P-Channel JFET

Features

- InterFET [P0099F Geometry](#)
- Low noise: 1.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @10V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

Industry Standard Crosses

- TBD

InterFET Similar Parts

- 2N5114-5-6
- J174-5
- P1086-7
- U304-5-6

InterFET Dual Parts

- TBD

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

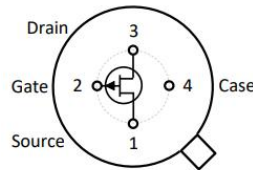
Description

The 25V InterFET IFN3993/A and IFN3994/A are targeted for choppers and high-speed commutator designs. The on resistance is typically less than 100 Ohms at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

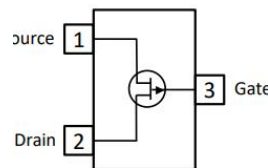
Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN3993; IFN3994 IFN3993A; IFN3994A	Through-Hole	TO-72	Bulk
PN3993; PN3994 PN3993A; PN3994A	Through-Hole	TO-92	Bulk
SMP3993; SMP3994 SMP3993A; SMP3994A	Surface Mount	SOT23	Bulk
SMP3993TR; SMP3994TR SMP3993ATR; SMP3994ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFN3993COT; IFN3994COT IFN3993ACOT; IFN3994ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN3993CFT; IFN3994CFT IFN3993ACFT; IFN3994ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

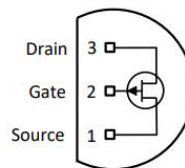
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



NOTE: Source and Drain pins are electrically interchangeable



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-72	SOT-23	TO-92	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG} Continuous Forward Gate Current	50	50	50	mA
P_D Continuous Device Power Dissipation ¹	500	350	500	mW
P Power Derating ¹	3.3	2.8	4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

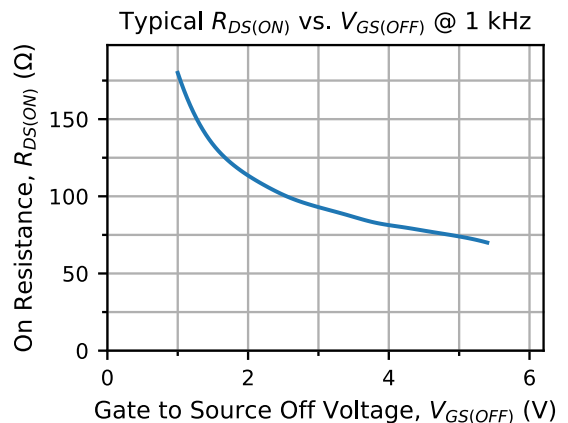
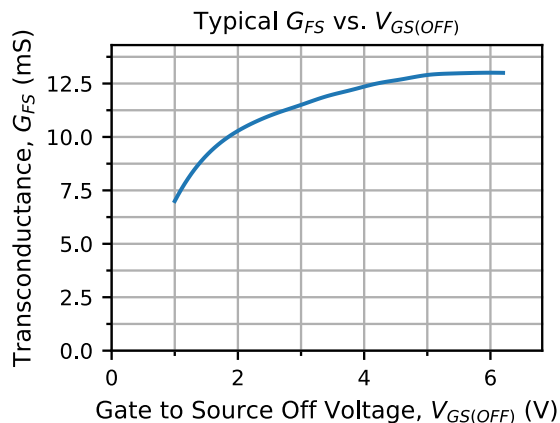
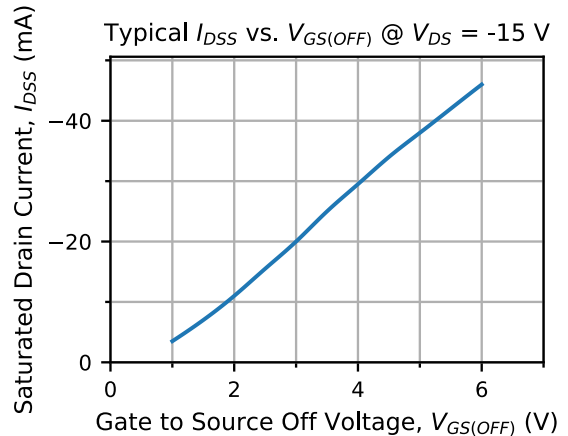
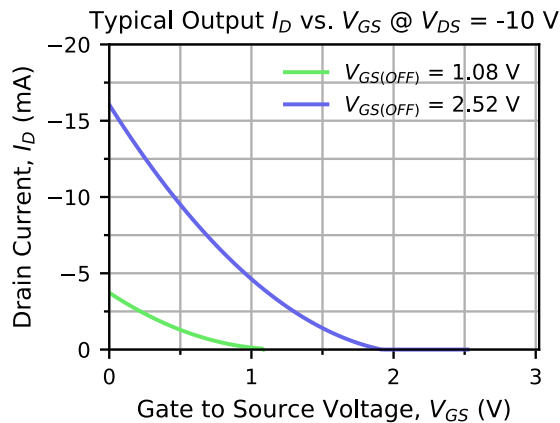
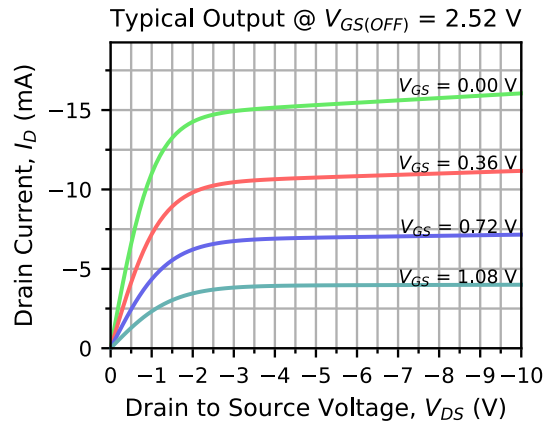
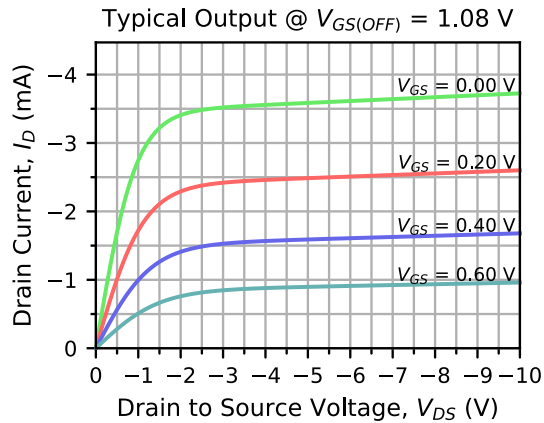
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	IFN3993/A		IFN3994/A		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = 1\mu A$	25		25		V
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = -10V, I_D = -1\mu A$	4	9.5	1	5.5	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = -10V$ (Pulsed)	-10		-2		mA
I_{DGO} Drain Reverse Current	$V_{GS} = -15V, I_S = 0A, T_A = 25^\circ\text{C}$		-1.2		-1.2	nA
	$V_{GS} = -15V, I_S = 0A, T_A = 150^\circ\text{C}$		-1.2		-1.2	μA
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = -10V, V_{GS} = 10V, T_A = 25^\circ\text{C}$		-1.2		-1.2	nA
	$V_{DS} = -10V, V_{GS} = 10V, T_A = 150^\circ\text{C}$		-1		-1	μA

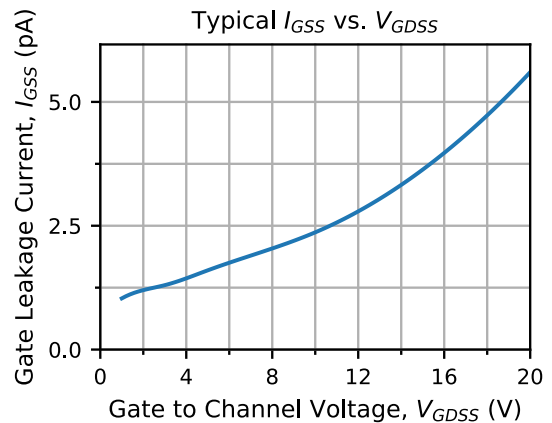
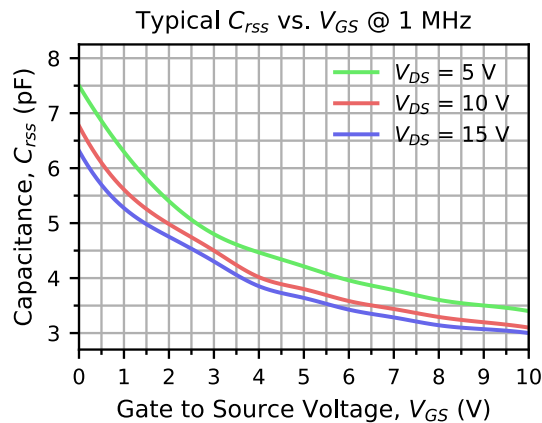
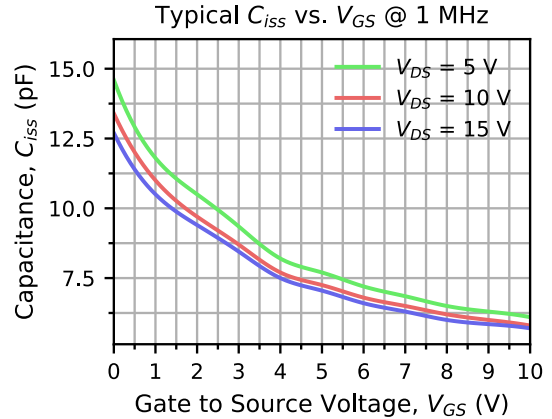
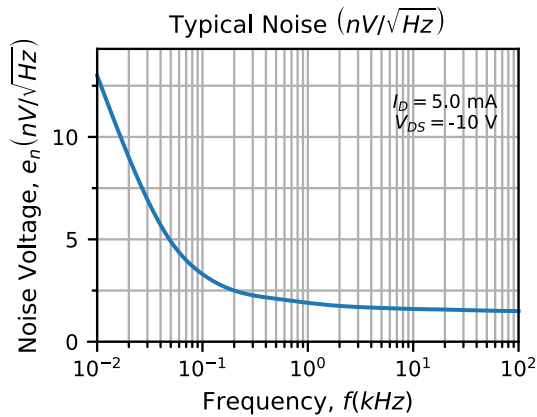
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	IFN3993/A		IFN3994/A		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = -10V, V_{GS} = 0V, f = 1\text{kHz}$	6	20	4	20	mS
		7	20	5	20	
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 0A, f = 1\text{kHz}$		150		300	Ω
C_{iss} Input Capacitance	$V_{DS} = -10V, V_{GS} = 0V, f = 1\text{MHz}$		16		16	pF
			12		12	
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 0V, V_{GS} = 10V, f = 1\text{MHz}$		4.5		5	pF
			3		3.5	

Typical IFN3993, IFN3994 Characteristics

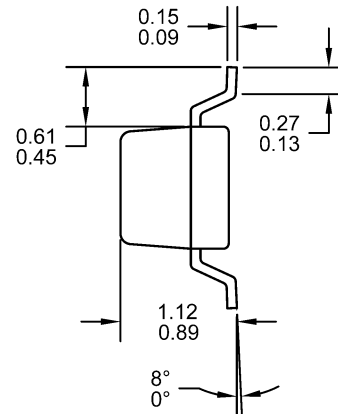
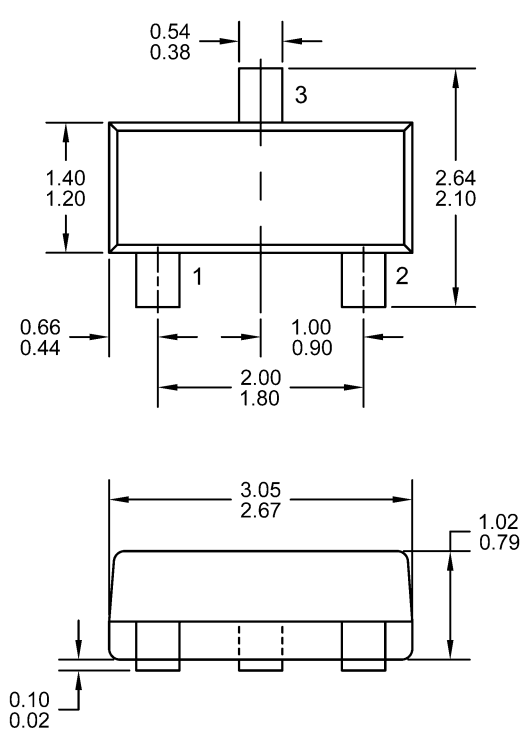


Typical IFN3993, IFN3994 Characteristics (Continued)



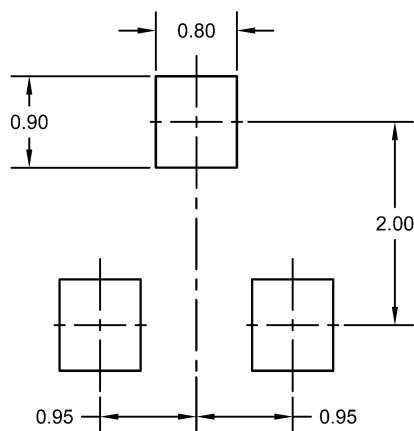
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

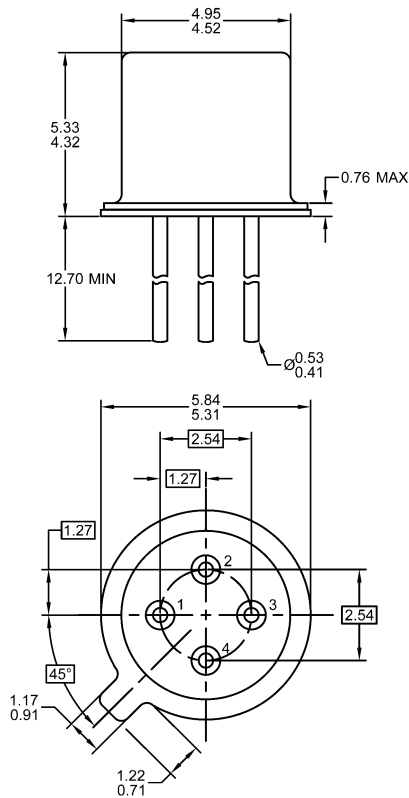
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

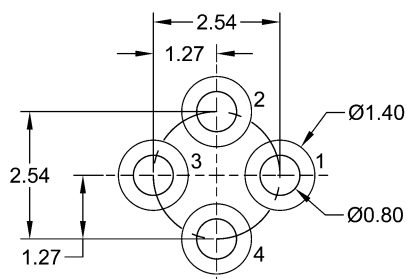
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

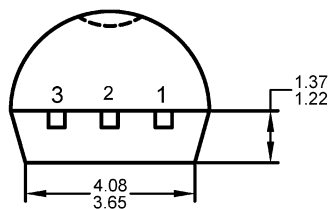
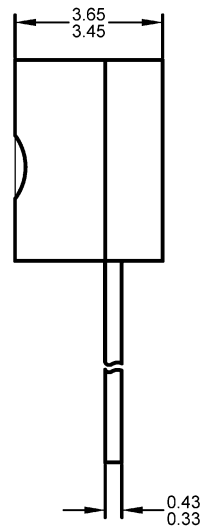
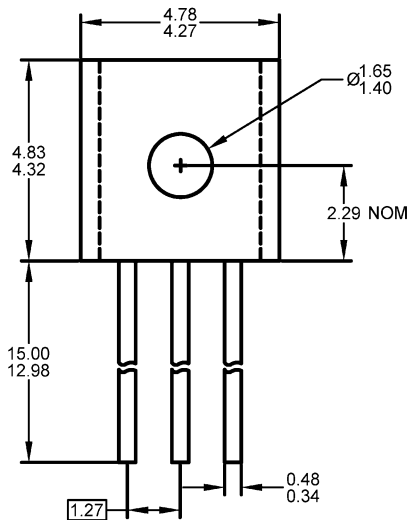
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

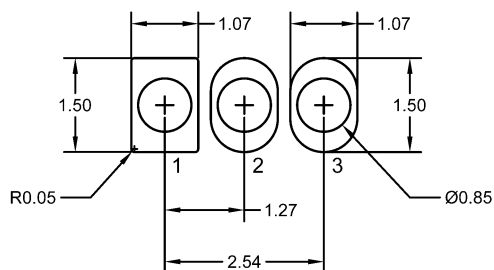
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

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