Application Note 107: Biasing JFETs to Achieve Zero Drift

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Introduction

For certain applications JFETs allow a simple means to achieve near-uniform performance over wide-ranging temperatures. The principle temperature effect on a silicon JFET affects the channel conductivity σ and the gate-to-channel junction barrier potential Ψ. As the temperature rises, both σ and Ψ decrease. This paper analyses this effect and identifies how a user may apply the principle to achieve near zero temperature-coefficient performance.

Analysis

The operating drain current, transconductance, and channel resistance are dramatically affected by temperature. As the temperature increases the movement (mobility) of majority carriers within the channel is inhibited. For both n- and p-type silicon, the variation of conductivity generally falls between 0.6 %/°C and 0.8%/°C.

The second factor affected by temperature that lends to this analysis is the change attributed to the gate-to-channel depletion region. Any reverse-biased pin junction exhibits a barrier potential depletion width that decreases with increasing temperature. As a consequence, with rising temperature, this decreasing barrier potential appears as a positive temperature coefficient of drain current. The gate-to-channel junction of a JFET exhibits exactly the same temperature coefficient as does the silicon junction bipolar transistor: -2.2 mV/°C.

As would be expected as channel conductance decreases, the drain current also decreases. But, as the gate-to-channel barrier potential decreases, the drain current increases. Obviously for the JFET to exhibit zero drift over temperature, the effects of decreasing channel conductance and a decreasing barrier potential must cancel.

Cobbold[1] offers the following derivations that allows us to resolve how to achieve the desired zero temperature coefficient.

With a JFET operating in saturation region, we can define drain current I_D by,

$$I_D = I'_D(\Psi, \sigma)$$

which, on differentiation yields,

$$\frac{dI_D}{dT} = \frac{\delta I'_D}{\delta \Psi}\frac{d\Psi}{dT} + \frac{\delta I'_D}{\delta \sigma}\frac{d\sigma}{\delta T} \qquad (2)$$

However, $\delta I'_D/\delta\Psi = g'_M$ when $I_D \propto \sigma$, so Equation (2) becomes,

$$\frac{dI'_D}{dT} = g'_M\frac{d\Psi}{dT} + \frac{I'_D d\sigma}{\sigma dT} \qquad (3)$$

Substituting 0.7% for $d\sigma/dT$ and 2.2mV/°C for $d\Psi/dT$ into Equation (3), the condition for zero-temperature coefficients becomes,

$$\frac{I'_{DZ}}{g'_{MZ}} = 0.315\ Volts \qquad (4)$$

This value is close to that observed in practice where the range usually lies within the range 0.29 to 0.33.

Taking Shockley's power law equation for double-diffused FETs,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSOFF}}\right)^2 \qquad (5)$$

and the equation for transconductance,

$$g_{fs} = 2\frac{I_{DSS}}{V_{GSOFF}}\left(1 - \frac{V_{GS}}{V_{GSOFF}}\right) \qquad (6)$$

We divide (5) by (6); then substituting into (4) we arrive at,

$$V_{GSOFF} - V_{GS} = 0.63\ Volts \qquad (7)$$

This equation identifies that value of V_{GS} that will give zero drift when the gate-source cut-off voltage is known. We see that for a JFET with a gate-source cut-off voltage of 0.63V, zero drift will occur at V_{GS} = 0V when $I_D = I_{DSS}$.

Since $|V_{GSOFF}|$ normally lies within the range 1.0V < $|V_{GSOFF}|$ < 5.0V we see from equation (7) that the condition for zero temperature coefficient occurs when V_{GS} is close to the gate-source cut-off voltage.

With the JFET operating at zero drift,

$$I_{DZ} = I_{DSS}\left(\frac{0.63}{V_{GSOFF}}\right)^2 \qquad (8)$$

$$g_{MZ} = g'_{FS}\left(\frac{0.63}{V_{GSOFF}}\right) \qquad (9)$$

Should the JFET under consideration for operation at zero temperature-coefficient have a high V_{GSOFF}, its operating drain current I_D will be considerably less than its saturation drain current I_{DSS}. Likewise, for most JFETs the resulting transconductance may be too low to be practical.

Operating at drain currents other than I_{DZ} will result in a drift in V_{GS}^2,

$$V_{GSDRIFT} = 2.2mV/°\text{C}\left(1 - \sqrt{\frac{I_D}{I_{DZ}}}\right) \qquad (10)$$

Conclusions

The values of I_{DZ} and g_{MZ} are proportional to the size of the JFET as defined by its geometry. For the 2N4117/A family we might anticipate an I_{DZ} of 40-50uA, with an associated g_{MZ} of 50uS; for the 2N4338 family an I_{DZ} of 300uA and a g_{MZ} of 500uS; and for the 2N4393 series an I_{DZ} closer to 3mA with a g_{MZ} in the area of 5mS.

When operating a JFET below its zero temperature coefficient, as the temperature rises both drain current and transconductance also rise. Above the JFET's temperature coefficient the opposite holds true.

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1. Richard S. C. Cobbold, *Theory and applications of Field-Effect Transistors*, ©1970 John Wiley & Sons, §3.7.2 "Effects of Temperature on the Channel," pp. 121-128.
2. *Designing With Field-Effect Transistors*, 2nd ed., revised by Ed Oxner, ©1990 McGraw-Hill, Inc.