Application Note 105: Improved Process for Manufacture of Radiation Hard N-Channel JFETs for Detector Electronics

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Introduction

Input transistors for SSC cryogenic calorimer preamplifiers must have very good low noise performance while remaining tolerant to the high radiation found inside the calorimeter near the interaction region. N-channel Junction Field Effect Transistors (JFETs) combine the best features of low noise operation and high tolerance to radiation to a greater extent than bipolar or MOS transistors. New designs and manufacturing methods are described which reduce the degradation of JFET noise performance due to neutrons. Two basic premises governed the choice of design and manufacturing methods. First, the JFET was designed with smaller features and spacings in order to minimize silicon in the active volume of the transistor. This reduces the interaction cross section with neutron radiation. Second, reduced feature size should increase the transconductance of the transistor, thereby improving noise performance.

Description of Experiment

The object of this study was to explore new designs and wafer fab processes to minimize the transistor dimensions. The most important goals were to reduce channel volume and increase transconductance of the JFET. The reduction of channel volume would reduce the degradation of the signal-to-noise ratio of the system due to lattice damage from neutrons. Increasing g_m/C ratio by increasing the device g_m is favored for the calorimeter application since total input capacitance is largely governed by the detector. The process also involved the use of thin oxides for passivation. It has been shown by Watanabe, et. al.,[1 & 2] that the use of very thin oxides and double dielectric layers can be used to reduce the effects of ionizing radiation. Also, a suitable guard ring structure was included to prevent the formation of parasitic inversion layers. Dopant concentration at the silicon/oxide interface at the conclusion of processing is designed to exceed the critical amount of $1 \times 10^{18}/cm^{-3}$ to prevent inversion from ionizing radiation (Sandia National Laboratory, Albuquerque[3]).

To accomplish these goals, a test matrix of both JFET design parameters and silicon epitaxy specifications was formed. The wafer fabrication process was developed to minimize lateral and vertical device dimensions. Several custom wafer lots were run to define the fabrication process. After this was successfully completed, a suitable wafer was identified from the final lot and samples were fabricated in TO-18 metal case packages. Their electrical and noise performance was measured and characterized as a function of the design parameters. Finally, these results were compared to standard production JFETs.

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Design Issues

The design matrix consists of sixteen combinations of gate-width and S/D pitch dimensions. These range from about 50-100% of the typical production JFET design rules. With the emphasis on those transistors with reduced dimensions, the test structures were loosely termed short-channel FETs, or SCFETs, to distinguish them from production type JFETs. A standard interdigitated structure was chosen with multiple source, gate and drain stripes repeated on a common centerline spacing, or pitch. This was implemented by designing a photomask set with four cells in an array. The cells each have four JFETs with a given gate-width and four different gate-lengths and S/D pitch. The four gate-widths were chosen to be similar to existing, production InterFET designs: NJ26, NJ72, NJ99, and NJ132 (See Table 1).

Table 1

Array Device	Gate-Width (um)	Comparable InterFET Device
Cell ”660”	660	NJ26 (2N4416)
Cell ”1800”	1800	NJ72 (U310)
Cell ”2500”	2500	NJ99 (U310 Modified)
Cell ”3350”	3350	NJ132 (2N6451 & IF1320)

Four JFETs are present in each cell sharing the common gate-width. These have a selection of gate-length and S/D pitch that is described in Table 2. The 8 and 10 micron S/D pitch designs are both considerably tighter than the normal InterFET production process. In addition, the 1.5 micron line width used for the gate and S/D stripes is smaller than the normal negative photoresist process would allow. The object was both to bound the standard production design dimensions, and to push the limits tighter than existing InterFET product designs.

Table 2

Design Gate-Length (um)	S/D Pitch (um)
5.0	20
3.5	15
2.5	10
1.5	8

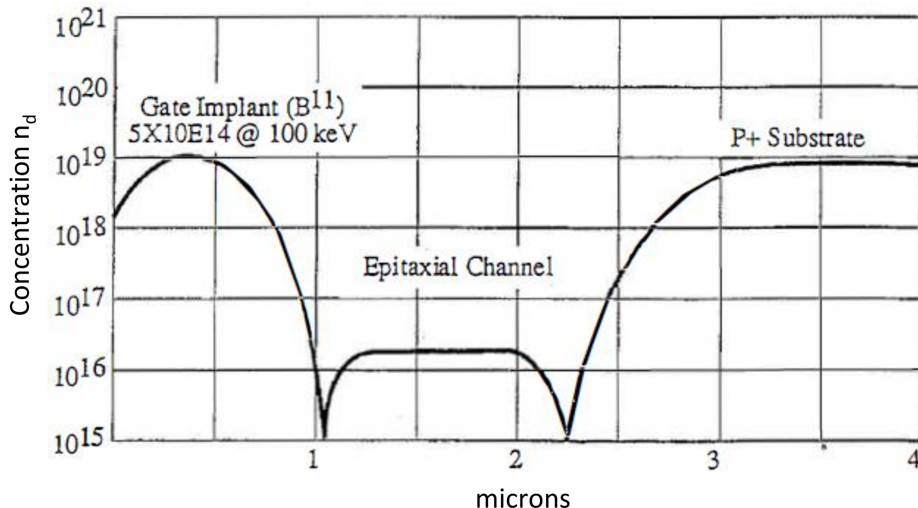
Wafer Process

The wafer process flow was similar in the basic concept to the standard process used at InterFET, but differed in specification requirements, control of critical dimensions, and methods to introduce dopants to form the transistor structures. The process involved the use of an n-type (phosphorus) epitaxial layer over a heavily doped p-type (boron) substrate. The epitaxial layer forms the channel of the JFET, and the p-type substrate forms the backside gate, or lower boundary defining the channel. This produces an n-channel JFET whose principle structures are diffused into the epitaxial layer.

The object of the newer design is to end up with the proper selection for the electrical parameters, but with much smaller design features. This has the greatest impact upon the gate pinch-off voltage, V_P, and breakdown voltage, BV_{GSS}. Very tight features and spacings means that the effects of diffusion, both lateral and vertical, must be very carefully controlled and minimized. Lateral diffusion affects all the silicon structures defined by photomasks and vertical diffusion is important to control junction profiles from the surface, and up from the highly doped substrate.

The wafer fabrication process was chosen to minimize junction diffusion. Ion implantation rather than high-temperature gas deposition was used to dope the silicon. Boron was implanted for both the guard ring and gate structures. Phosphorus was implanted to form the S/D overdope regions. The starting epitaxial silicon thickness was chosen to allow a minimum amount of implant anneal and total junction diffusion during processing. The initial thermal oxidation thickness was 2500 angstroms, about a third of the normal production process. This reduces both the diffusion of the heavily doped substrate up into the channel, and the sensitivity to ionizing radiation. The desired junction profiles of the key transistor features are shown in Figure 1.

Figure 1. Profile of Gate Implant Into Epitaxial Silicon



An assumption was made that better noise performance would be achieved by the use of an epitaxially formed channel for the transistors. This was based upon the fact that an epitaxial layer has only a single species of dopant atoms, which can be controlled to obtain a relatively uniform doping profile independent of the substrate silicon. Conversely, a channel formed by diffusion must reverse the starting polarity type by adding a greater number of dopant atoms (compensation) to the lattice. In addition, if an implant process is used to form the channel, further lattice damage is likely.

It was necessary to specify a thinner layer of epitaxial silicon in order to minimize both lateral and vertical junction diffusions. Five different channel resistivities were used to determine possible effects on performance after radiation; 0.25, 0.5, 1.0, 1.6, and 5.0 ohm-cm target values. In each case two different thicknesses were used to increase the chance for the proper match of final device characteristics for the least amount of total processing diffusion. Thicknesses were targeted to achieve 2.0 and 2.5. microns of "flat zone" in the doping profile prior to wafer fabrication.

Results

Two-dimensional modeling was used to reduce process development time. Even so, several wafer fabrication lots were necessary to achieve the proper final device electrical parameters. The actual device doping profile turned out to be very close to that shown in Figure 1. It is important to note that the combination of channel doping concentration and distance between the top and back (lower) gate structures determines the transistor pinch-off voltage (V_P) - a fundamental control parameter in the process. It was found that the transistor pinch-off voltage was very sensitive to variations in the epitaxial thickness. Only one combination of epitaxy resistivity and thickness yielded the relatively low values of V_P that was desired among the tests run. Among two fab lots, four epitaxy groups resulted in V_P ranging from 1.4 to 12.0 V, indicating the sensitivity to starting epitaxy thickness. Besides achieving electrical parametric results, the wafer fab process also needed to provide suitable resistance to inversion of the guard ring under prolonged irradiation. Spreading resistance profiles on some of the wafers indicated that the minimum required concentration of $> 1 \times 10^{18}/cm^2$ was achieved.

Electrical and Device Characterization

The best match to desired electrical parameters was from the silicon epitaxy group with resistivity equal to 1.1 Ω-cm. This range of resistivity is typical for the manufacture of a general purpose JFET. A channel resistivity of 0.25 to 0.50 Ω-cm would be a better choice to counter neutron damage effects due to higher dopant concentration. In addition, standard production experience would predict that 0.50 Ω-cm resistivity should increase g_m around 25%. Somewhat surprisingly, even the devices made with the tightest spacings yielded good functioning JFETs. As expected, both I_{DSS} and gain improve significantly as the gate-length/pitch is reduced. Also, both V_P and g_m increase with decreasing gate-length/pitch. The change is rather large between the two tightest spacings, indicating, perhaps, that we were near the minimum workable limit for this process/material combination.

Figure 2. Transconductance versus Pitch for SCFET Families

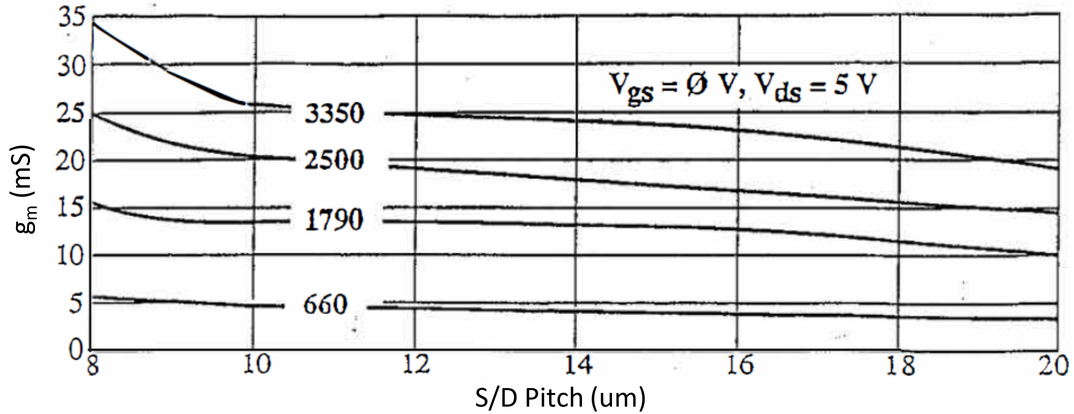
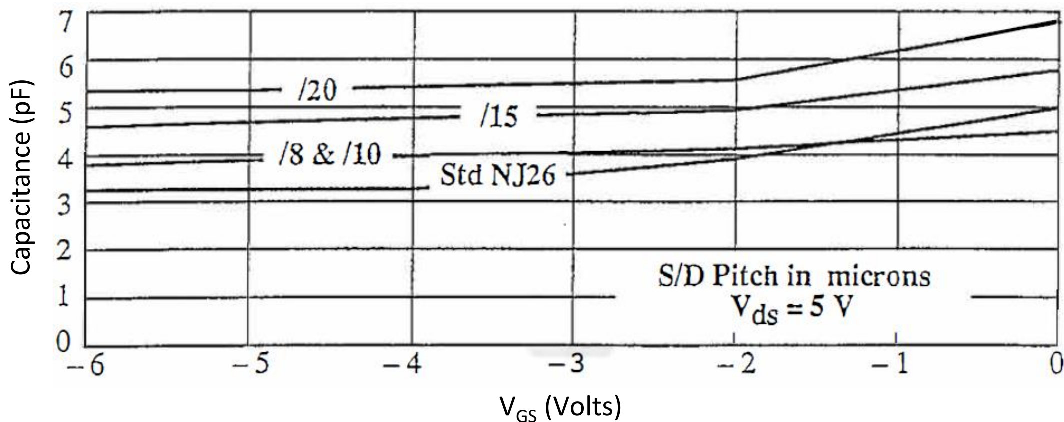


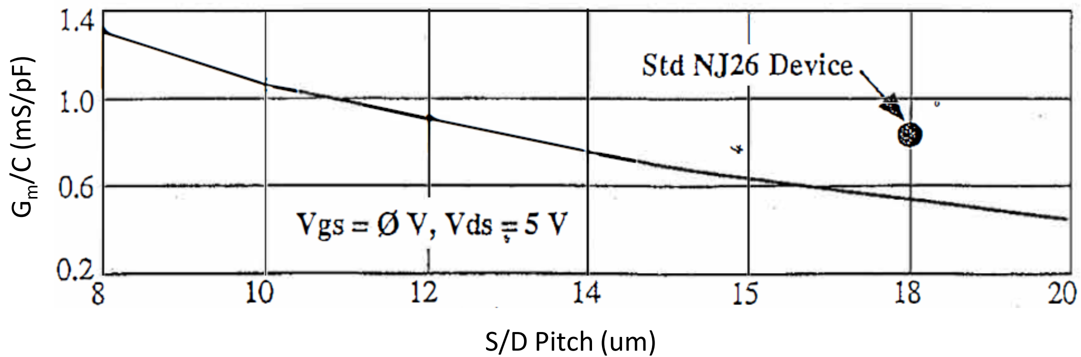
Figure 2 shows g_m as a function of S/D pitch for each of the four gate-widths. As expected, g_m increases for greater gate-width and reduced pitch. Evidence of the minimum spacing limit was also seen on the breakdown voltage. There is a bi-modal distribution of BV_{GSS} as pitch is changed from 10 to 15 microns. The two wider spacings have approximately 25V BV_{GSS}, while the two tighter designs run around 12-15 V.

Figure 3. Input Capacitance versus Gate Voltage. SCFET 660 Family



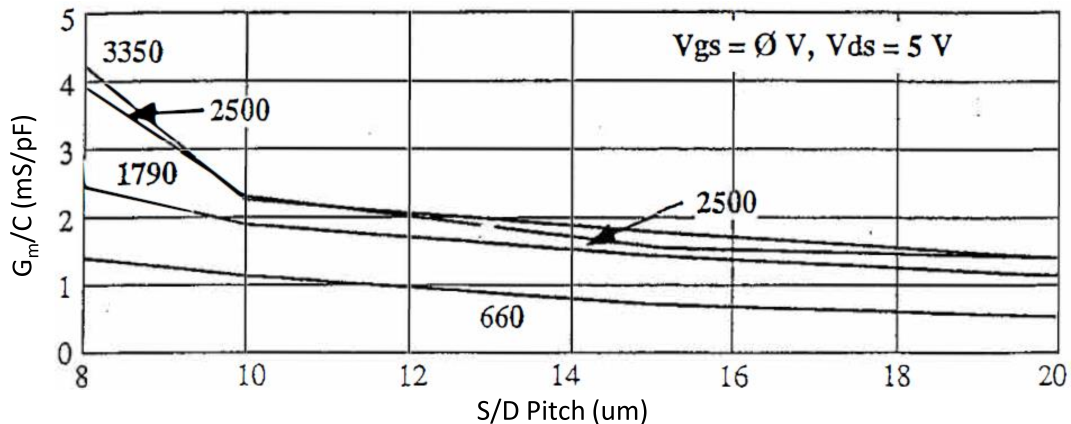
In Figure 3 input capacitance is plotted against VGS for the 660 micron gate-width family of JFETs. Notice that the characteristic curves are somewhat flatter than the production NJ26 JFET (same gate-width and S/D pitch of 18 microns).

Figure 4. g_m/C Ratio. SCFET 660 Family



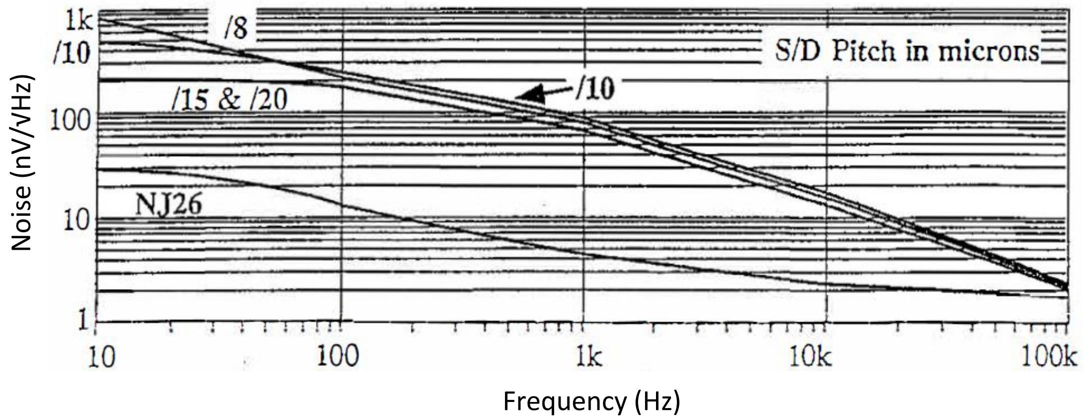
High g_m/C ratio is important for good noise performance and high switching speeds. In Figure 4 g_m/C is shown for the 660 micron family as a function of S/D pitch. As expected, the highest g_m/C occurs for the tightest spacings. The NJ26 production part, with similar channel resistivity, falls somewhat above the curve of the SCFETs.

Figure 5. g_m/C Ratio. SCFET Family



In Fig. 5 the g_m/C vs. pitch curves are shown for all four gate-width cases. The g_m/C ratio improves with increasing gate width. This is probably due to the more efficient use of active transistor area in the larger designs. There is a small, fixed separation (necessary for adequate breakdown voltage) between the end of each S/D finger and the adjacent isolation guard ring. The larger gate width devices use longer gate stripes, which means that these end effect losses are reduced.

Figure 6. Noise versus Frequency. SCFET 660 Family



A very interesting result is shown in Figure 6, which plots room temperature equivalent noise performance, e_n, as a function of frequency and compares the test JFETs to the similar NJ26 production device. At very low frequency (10Hz) the 8 and 10 micron gate lengths are considerably noisier than the 15 and 20 micron JFETs. However, for frequencies in the range 100 to 100 kHz there is not much difference. Also, the standard NJ26 JFET is as much as 30 times less noisy than the short-channel JFETs at 10Hz, but is only about twice as good at f = 100kHz. This difference is apparently due to the difference in the basic process, particularly the use of ion implantation to form the transistor structures in the test JFETs.

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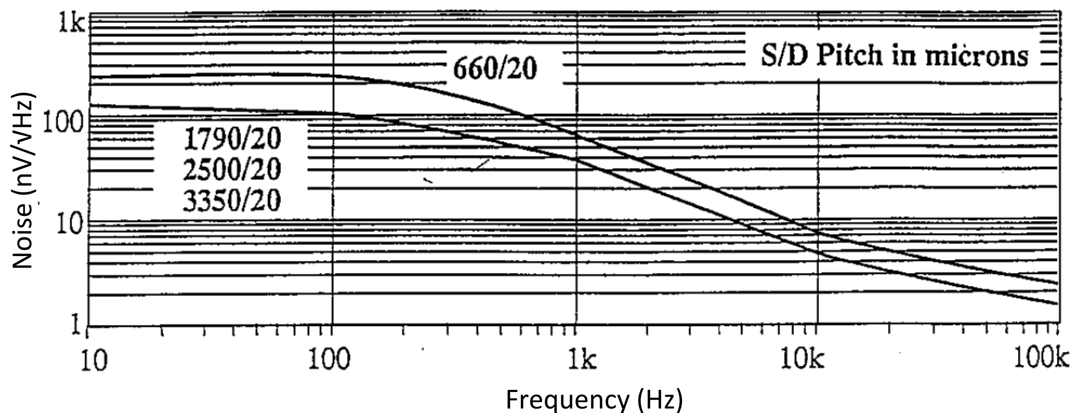
Figure 9. SCFET Noise versus Frequency Best Case of Each Gate-Width



The noise performance which compares the best case for each gate-width is shown in Figure 9. There is not much difference for the three largest gate-width cases. There is a fairly uniform increase in noise of the 660-micron case by about 2X over the other three part families. The reason for the difference is not clear, but may be due to the S/D finger end effects that were mentioned previously.

Summary

The results of the SCFET project have been very encouraging. A process which uses a very thin, epitaxially formed channel and ion implantation to form the isolation, gate, and source/drain regions has been demonstrated. The precision of the epitaxial thickness appears to be an area which could greatly affect gate targeting and process yields of the production process. Improved methods of manufacturing thin silicon epitaxy would be a great benefit. The reduced device line widths will require the use of a tightly controlled, positive-photoresist process, or more sophisticated direct write photolithography. The achievement of better JFET performance and higher production yields will require production control improvements in both thin-film epitaxy and fine-line photolithography.

Electrical results are also very positive. Electrical gain and g_m/C performance can be significantly improved by reducing gate length and S/D pitch. The g_m and g_m/C ratio were improved by up to 50% and 400%, respectively, for the 3350 micron gate-width over the equivalent, standard production JFETs. The equivalent noise performance is improved as the device gate width is increased. Noise performance is less sensitive to changes in pitch dimension, but the tightest 8-micron spacing is somewhat noisier in all cases. This could indicate the onset of hot electron injection. The 8 and 10 micron pitch cases also showed reduced BV_{GSS}, to around 10V to 12V, which must be considered in the circuit design.

Compared to the equivalent, production JFETs, the noise performance of the short-channel JFETs is significantly worse for frequencies in the range of 10Hz-10kHz. However, at f = 100 kHz equivalent noise is within 50% of the production JFETs. Since SSC applications require very short signal processing times, there may not be much noise penalty. At this time SCFET performance with respect to radiation hardness is not available, but the results are expected to be favorable. SCFET prototypes are currently being evaluated by Brookhaven National Laboratory to determine whether the reduced channel volume will result in less noise degradation due to neutron radiation compared to the currently available JFETs.

Acknowledgements

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