Application Note: InterFET Thermal SOIC-8 Package

While other JFET manufacturers produce monolithic dual JFETs on a single substrate, closely placed together for better temperature coefficients and matching, InterFET separates the JFETs by 0.56 millimeters; this creates adjacent die that are matched pairs. The benefit of this approach is lower crosstalk noise between the two monolithic JFETs. When both JFETs are on the same monolithic substrate, a parasitic bipolar transistor is created by the substrate which causes current to flow between the JFETs and appear as noise. InterFET matches adjacent die to stringent electrical characteristics to eliminate the parasitic transistor as a source of noise. By using adjacent die, the temperature coefficients and matching are still very well preserved.

In order to further optimize the thermal performance of InterFET dual JFETs a customized SOIC-8 package was developed. This package requires two pins connected to the gate substrate to thermally optimize removing the heat from the JFET die. The 2 gate substrate pins allow for an optimized PCB thermal pad to remove the JFET package heat.

Figure 1 to the right is the pinout for an SOIC-8 dual JFET package. This pinout differs from other JFET manufacturers but can be compensated for with a dual layout option as illustrated in figure 2 below. As seen in figure 2 the PCB thermal pads can be placed to the top and the bottom of the SOIC-8 package while maintaining a dual footprint layout.

Figure 1 – IF389A, B, C, D Pinout

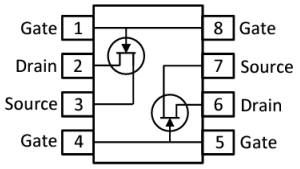

Figure 2 – Dual layout IF389 and LSK389