

2N6550 N-Channel JFET

Features

- InterFET [N0450L Geometry](#)
- Low noise: 1.0 nV/VHz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @10V
- Low $V_{GS(OFF)}$: -1.0 typical
- Typical I_{DSS} : 12mA
- Typical BV_{GSS} : -35V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

Industry Standard Crosses

- TBD

InterFET Similar Parts

- IF4500

InterFET Dual Parts

- IFN860

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

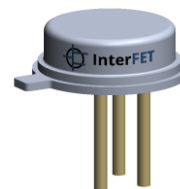
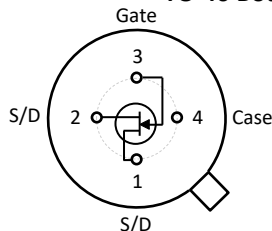
Description

The -20V InterFET 2N6550 is targeted for sensitive amplifier stages for mid-frequencies designs. The 2N6550 has a cutoff voltage of less than 3.0V ideal for low-level power supplies. The TO-46 package is hermetically sealed and suitable for military applications.

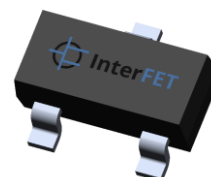
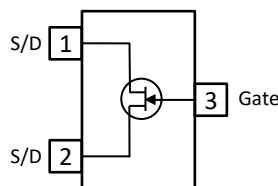
Ordering Information

Part Number	Description	Case	Packaging
2N6550	Through-Hole	TO-46	Bulk
PN6550	Through-Hole	TO-92	Bulk
SMP6550	Surface Mount	SOT23	Bulk
SMP6550TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N6550COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N6550CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

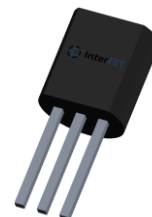
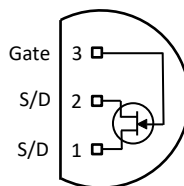
TO-46 Bottom View



SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-46	SOT-23	TO-92	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG} Continuous Forward Gate Current	50	50	50	mA
P_D Continuous Device Power Dissipation ¹	500	350	500	mW
P Power Derating ¹	3.3	2.8	4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

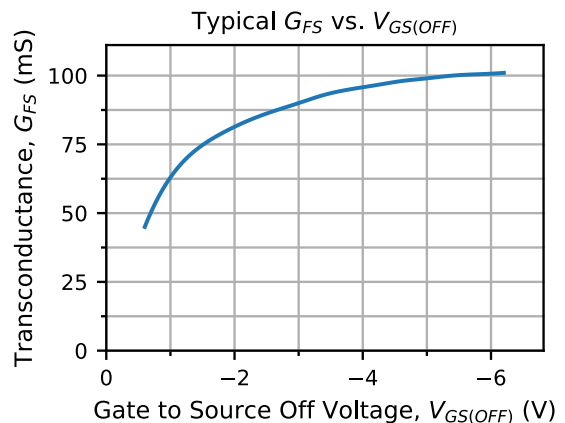
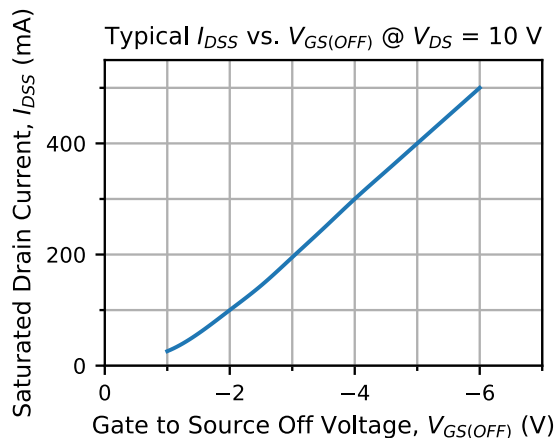
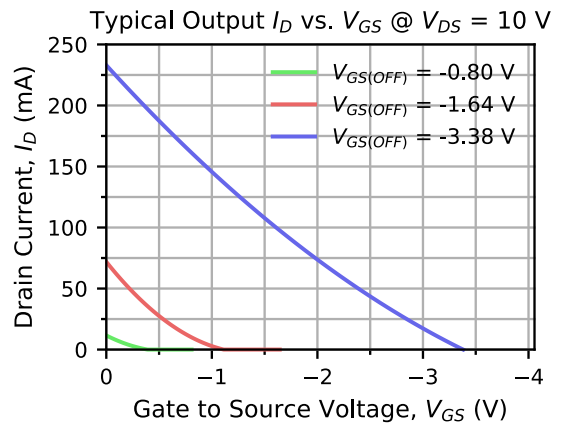
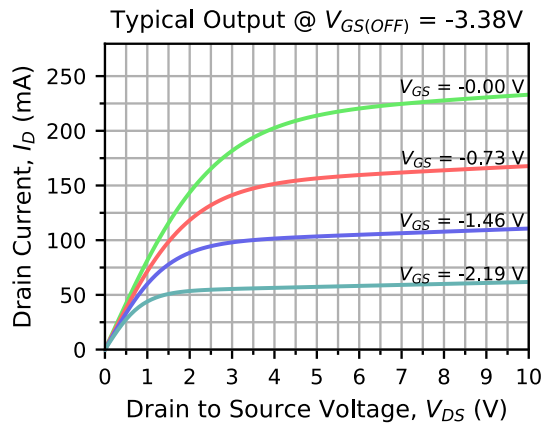
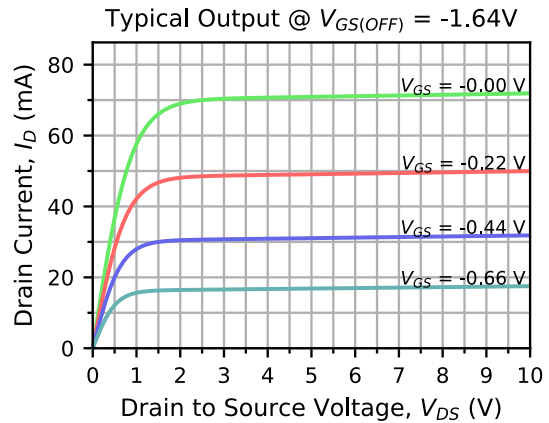
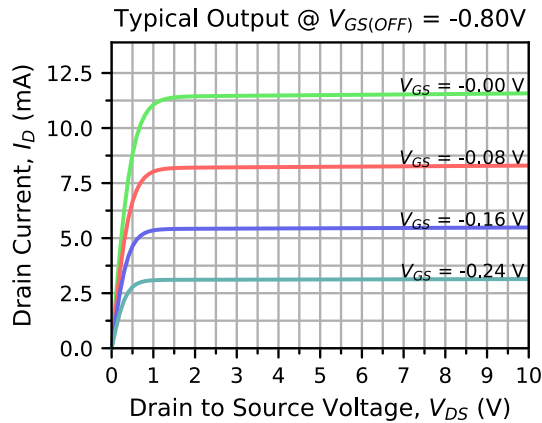
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N6550			Unit
		Min	Typ	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = 10\mu A$	-20			V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -10V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -10V, V_{DS} = 0V, T_A = 85^\circ\text{C}$			-3 -0.1	nA μA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 0.1mA$	-0.3		-3	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	10	100	250	mA

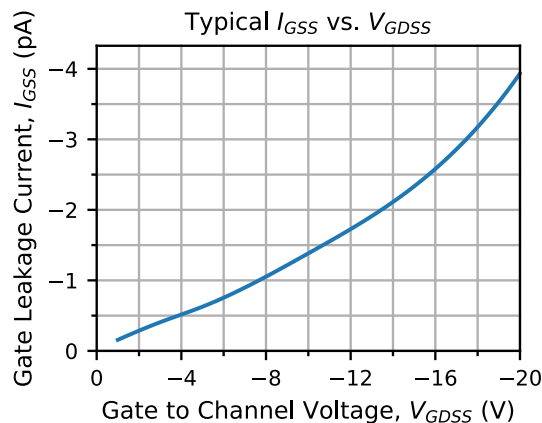
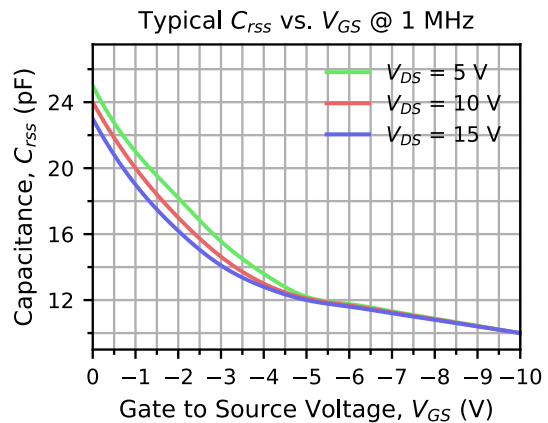
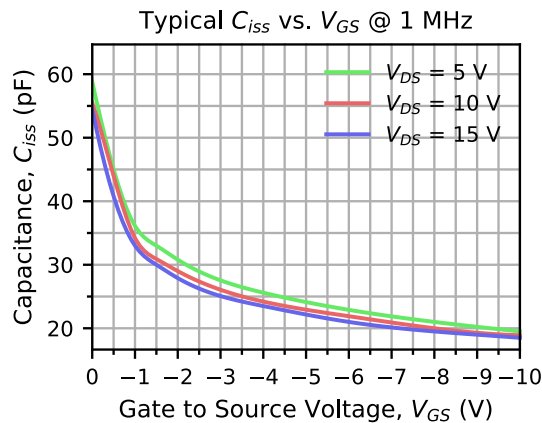
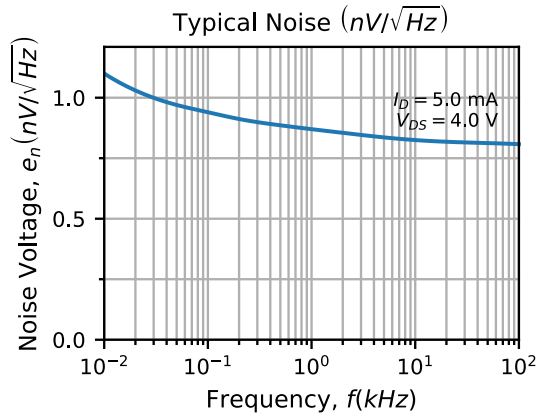
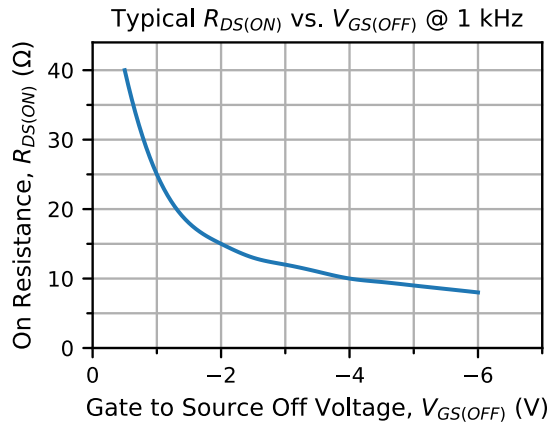
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N6550			Unit
		Min	Typ	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10V, I_D = 10mA, f = 1kHz$	25		150	mS
G_{OS} Output Conductance	$V_{DS} = 10V, I_D = 10mA, f = 1kHz$			150	μS
C_{iss} Input Capacitance	$V_{DS} = 10V, I_D = 10mA, f = 140kHz$		30	35	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 10V, f = 140kHz$		10	20	pF
e_n Equivalent Input Noise Voltage	$V_{DS} = 5V, I_D = 10mA, f = 10Hz$ $V_{DS} = 5V, I_D = 10mA, f = 1kHz$		6 1.4	10 2	nV/ \sqrt{Hz}
$e_{n \text{ Total}}$ Equivalent Total Input Noise Voltage	$V_{DS} = 5V, I_D = 10mA, f = 10kHz \text{ to } 20kHz$		0.4	0.6	μV_{rms}
i_n Equivalent Input Noise Current	$R_S < 100 k\Omega, f = 1kHz$		0.1		pA/ \sqrt{Hz}

Typical 2N6550 Characteristics

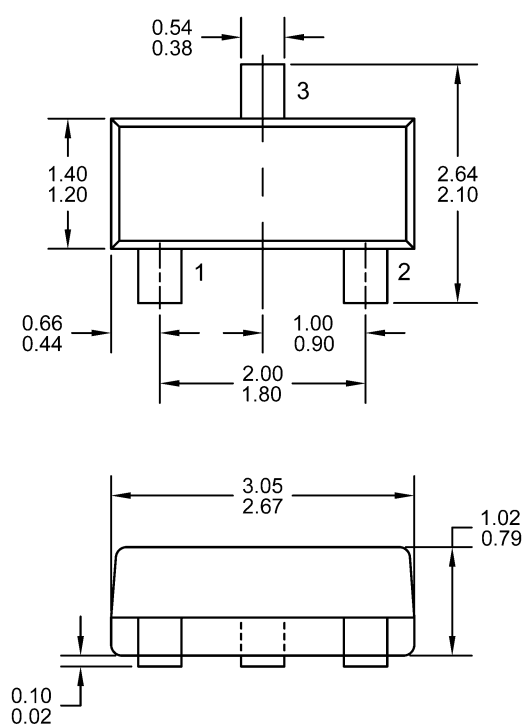


Typical 2N6550 Characteristics (Continued)



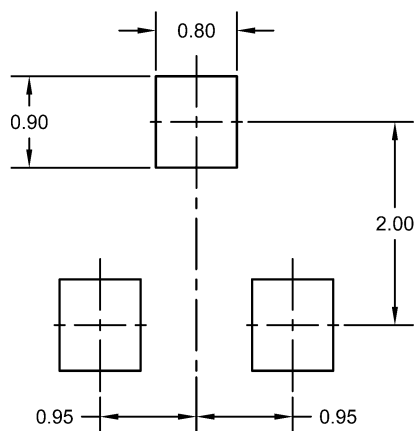
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

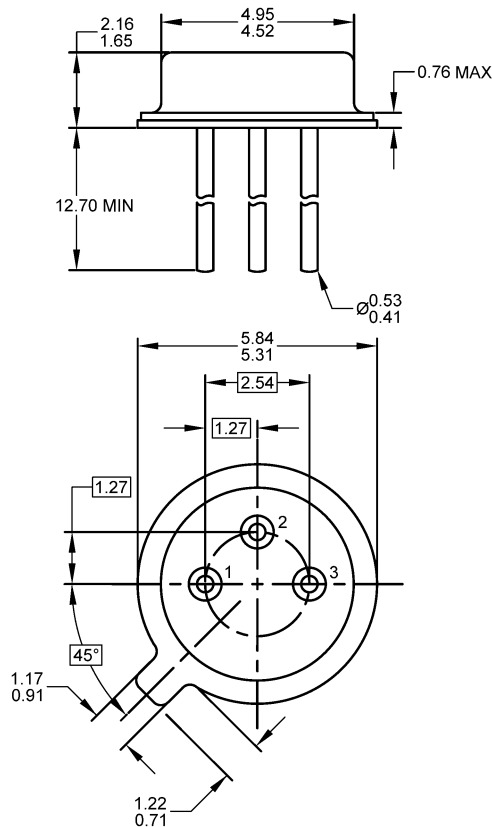
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

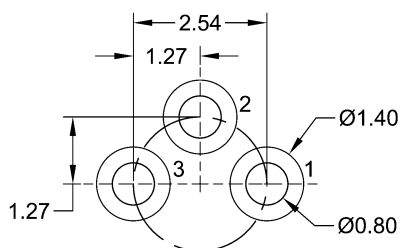
TO-46 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.23 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

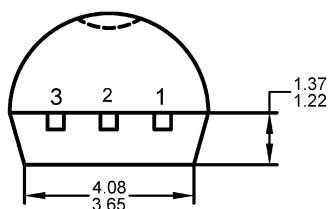
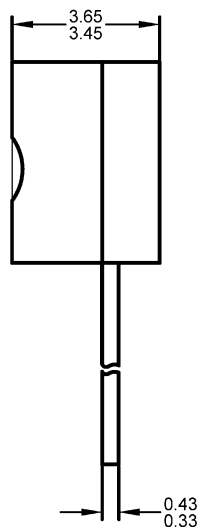
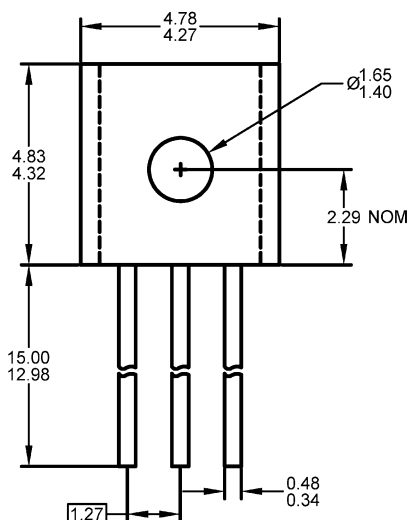
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

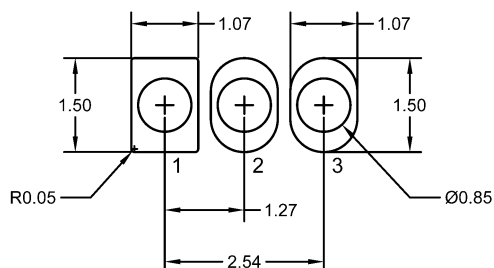
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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