Low Noise Front-End for HEP Experiments:
from the Brookhaven Years to the Road Ahead

In Memoriam of Franco Manfredi
1935-2015

Sergio Rescia
Brookhaven National Laboratory

Pavia, 5 December 2016

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Low Noise Front-End for HEP Experiments:

from the Brookhaven Years to the Road Ahead

A Symposium in Memoriam of

Franco Manfredi

Sergio Rescia
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Franco Manfredi: the Brookhaven Days

The Supercollider Days and the Monolithic JFET Preamplifier Project

… and its legacy

… and the future

Franco Manfredi

Circa 1987-88 at BNL …

DESIGN OF A CHARGE SENSITIVE PREAMPLIFIER ON HIGH RESISTIVITY SILICON

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ABSTRACT

A low noise, fast charge sensitive preamplifier was designed on high resistivity, detector grade silicon. It is built at the surface of a fully depleted region of n-type silicon. This allows the preamplifier to be placed very close to a detector anode. The preamplifier uses the classical input cascode configuration with a capacitor and a high value resistor in the feedback loop. The output stage of the preamplifier can drive a load up to $20pF$. The power dissipation of the preamplifier is $13mW$. The amplifying elements are "Single Sided Gate JFETs" developed especially for this application. Preamplifiers connected to a low capacitance anode of a drift type detector should achieve a rise time of $20ns$ and have an equivalent noise charge (ENC), after a suitable shaping, of less than 50 electrons. This performance translates to a position resolution better than $3\mu m$ for silicon drift detectors.

1. Introduction

A relatively new type of semiconductor detectors, Semiconductor Drift Detectors[1] have a very low anode capacitance. Typical values for multianode detectors and for large area cylindrical detectors are about $70fF$. This very small value of the detector capacitance should lead to a very low noise performance which was really observed[2]. Until now, however, tests were done using electronics constructed from the best commercially available discrete transistors. The input capacitance of the smallest available FET 2N 4416 is about $4pF$. The total input capacitance achieved with a 2N4416 FET as the first transistor was $6pF$. Thus there is a factor of 100 mismatch between the low output capacitance detector and the input capacitance of commercially available FETs.

The realization of the first amplification stage directly on the wafer of the detector has two advantages

1. the input transistor can be made small enough to match the small detector capacitance.
2. stray capacitances due to the connection between the detector anode and the first transistor can be kept at a minimum.

The realization of matched preamplifiers with a minimum stray capacitance should decrease the noise of the detector-preamplifier system, resulting in a substantial improvement of energy and position resolution of silicon drift detectors and fully depleted Charge Coupled Devices (CCDs).

For spectroscopic applications the estimated noise of a cylindrical large area drift detector operating at room temperature is about 50 electrons r.m.s. which corresponds to an energy resolution of $400eV$ FWHM.

A calculated position resolution for a multianode detector of an area of $4 \times 4cm^2$ is about $3\mu m$ in both, x and y direction. This resolution is a factor of three better than the resolution obtained up to now with a commercially available electronics and corresponds to 10^8 pixels achieved with only 500 read-out channels.

Fully depleted CCDs are realizable on the same type of high resistivity silicon material as drift detectors. The designed preamplifier or even a simple source follower realized from designed amplification elements on a fully depleted CCD should have an equal performance as the electronics on standard CCDs.

We believe that the calculated improvements in the performance of the drift detectors and fully depleted CCDs with an

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* This research is also supported by the Italian INFN and CNR.
** Also *MBB* GmbH

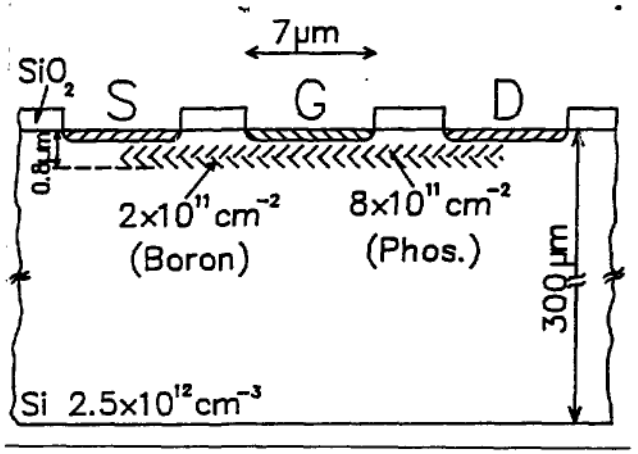

Fig. 3.1: Cross section of a "Single Sided Gate JFET". The gate is indicated by (G), source and drain by (S) and (D) respectively.

4. Charge Sensitive Preamplifier

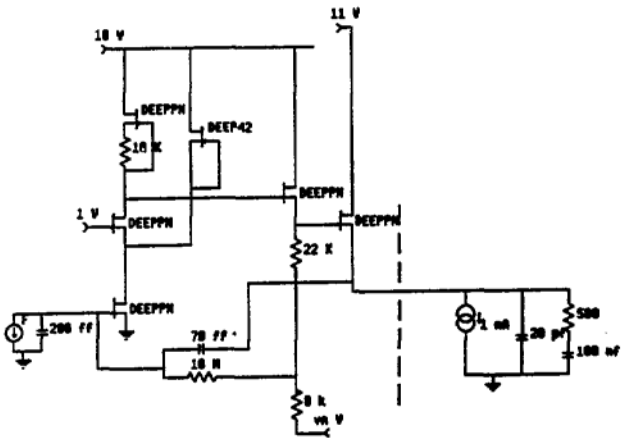

Fig. 4.1: Charge sensitive preamplifier on high resistivity silicon.

…. and in Milano.

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North-Holland, Amsterdam

Section VI. Signal processing and data acquisition

LOW NOISE MONOLITHIC CMOS FRONT END ELECTRONICS

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Design considerations for low noise charge measurement and their application in CMOS electronics are described. The amplifier driver combination whose noise performance has been measured in detail as well as the analog multiplexing silicon strip detector readout electronics are designed with low power consumption and can be operated in pulsed mode so as to reduce heat dissipation even further in many applications.

1. Introduction

With ever increasing size and granularity of high energy experiments and corresponding high numbers of identical readout channel being in the range of 10^4 to 10^6, it seems natural to employ custom designed integrated electronics in order to save money, space, and heat dissipation. This is especially important for colliding beam experiments where usually almost complete coverage of solid angle together with measurement close to the interaction vertex leave little space for electronics. Furthermore, in order to reduce the number of connections to the outside, local data storage and sequential readout seem to be important. The situation is extreme for silicon strip detectors which due to their capability of measuring charged particle tracks with a precision of a few μm are ideal vertex detectors. Here a desired readout pitch of 20–50 μm makes the use of conventional electronics nearly impossible.

With the present high standard of development of industrial microelectronics it might seem fairly simple to apply it to the needs of the high energy community. Although this is perhaps true for digital applications, low noise analog signal processing poses problems which are nonstandard for industry. It is the purpose of this paper to analyze these problems and show a way to solve them. This will be done following several projects which are presently under development in collaboration by the Max-Planck Institut für Physik and Astrophysik in Munich, the Fraunhofer Institut in Duisburg and since recently the Universities of Milano and Pavia. In order to facilitate a systematic presentation of these projects we will start with some general considerations concerning charge measurement, noise and signal processing before going into specifics concerning integrated electronics.

2. Charge sensitive amplifier

The well known principle of a charge sensitive amplifier is shown in fig. 1. It consists of an operational amplifier (amplification V_0) with a feedback capacity C_f which may be discharged by closing the reset switch. The detector, represented by its capacitance C_D, is connected to the inverting input. C_{in} represents the input capacitance of the amplifier, usually dominated by the input transistor. The output voltage

$$U_{out} = -\frac{Q_{in}}{C_f + \frac{C_D + C_{in} + C_f}{V_0}}$$

reduces to the obvious result $U_{out} = -Q_{in}/C_f$ for very large amplification V_0. The input of the circuit looks (for low frequencies) like a capacitor with

$C_{eff} = V_0 C_f + C_{in}$.

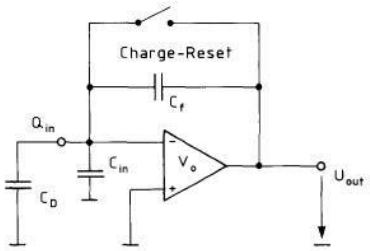


Fig. 1. Principle of a charge sensitive amplifier.

7. Conclusions

Custom designed integrated electronics, now only in the early stages, is expected to take over a dominant role in future experiments. Interesting and challenging technical problems exist especially in the analog front end part with the simultaneous requirement of low noise, low power, small size, high reliability and radiation hardness. Furthermore the integration of electronics and semiconductor detectors seems extremely interesting.

We have developed low noise-low power complementary metal oxide semiconductor (CMOS) electronics for several applications. Although this type of electronics with noise performance approaching that of good hybrid amplifiers may be adequate for most applications it has as any MOS electronics the unwanted properties of relatively large $1/f$ noise and of showing radiation damage at fairly low irradiation. Junction field effect transistors (JFETs) are known to have much lower $1/f$ noise and are expected to be radiation hard [7]. Therefore we have started to develop JFET electronics based on the CMOS compatible process developed at the Fraunhofer Institut in Duisburg [1].

Franco's Philosohy:

- Franco's background was in physics.
  He had a keen interest both in device physics and detector physics.

- He was a strong believer in the Milano group's (and Radeka's Instrumentation Division) philosophy that the only real optimization is of the detector – readout electronics as a whole, starting from first principles and basic device/detector properties.

Superconducting Super Collider

From Wikipedia, the free encyclopedia

The **Superconducting Super Collider** (**SSC**) (also nicknamed the **Desertron**[1]) was a particle accelerator complex under construction in the vicinity of Waxahachie, Texas.

Its planned ring circumference was 87.1 kilometers (54.1 mi) with an energy of 20 TeV per proton and was set to be the world's largest and most energetic. It would have greatly surpassed the current record held by the Large Hadron Collider which has ring circumference 27 km (17 mi) and energy of 6.5 TeV per proton. The project's director was Roy Schwitters, a physicist at the University of Texas at Austin. Dr. Louis Ianniello served as its first Project Director for 15 months.[2] The project was cancelled in 1993 due to budget problems.[3]

Contents [hide]

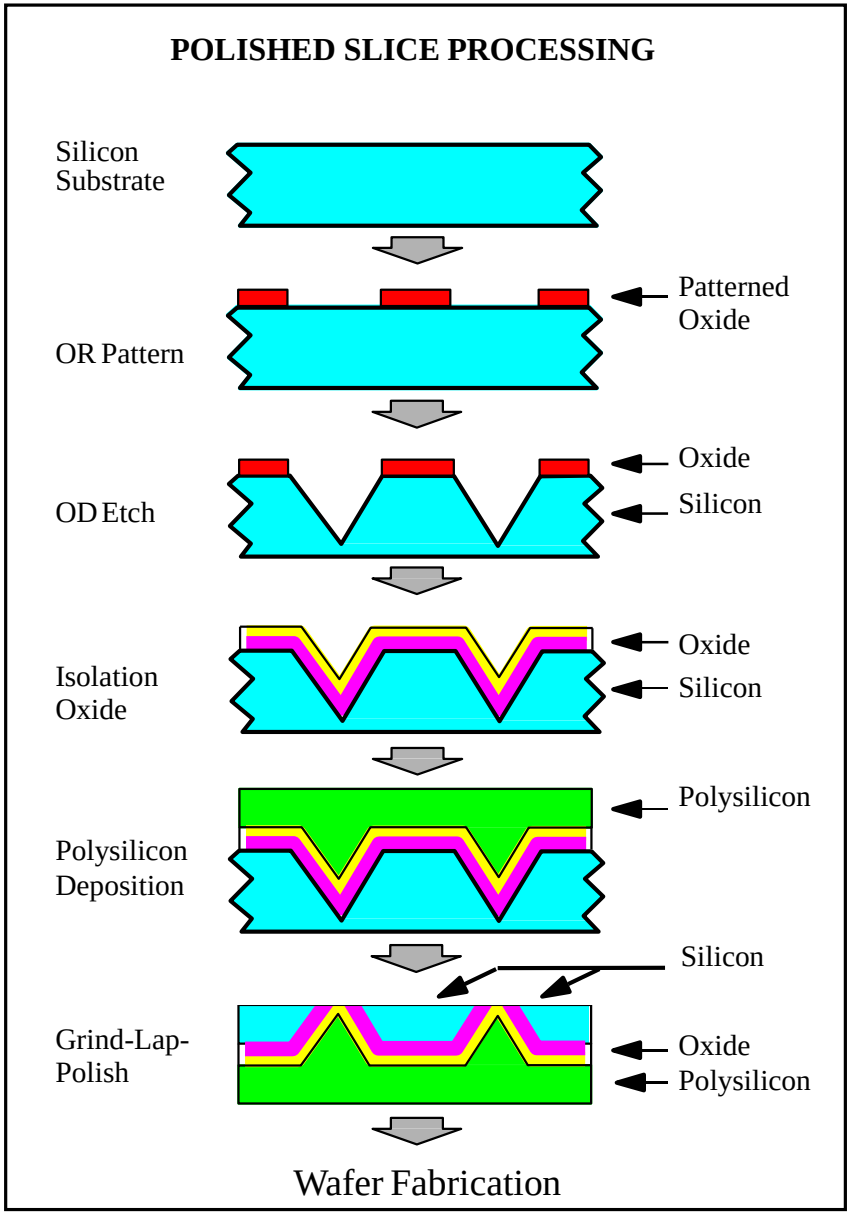
Proposal and development [edit]

The system was first formally discussed in the December 1976 National Reference Designs Study, which examined the technical and economic feasibility of a machine with the design capacity of 20 TeV per proton.[4] Fermilab director and subsequent Nobel physics prizewinner Leon Lederman was a very prominent early supporter – some sources say the architect[5] or proposer[6] – of the Superconducting Super Collider project, which was endorsed around 1983, and a major proponent and advocate throughout its lifetime.[7][8]

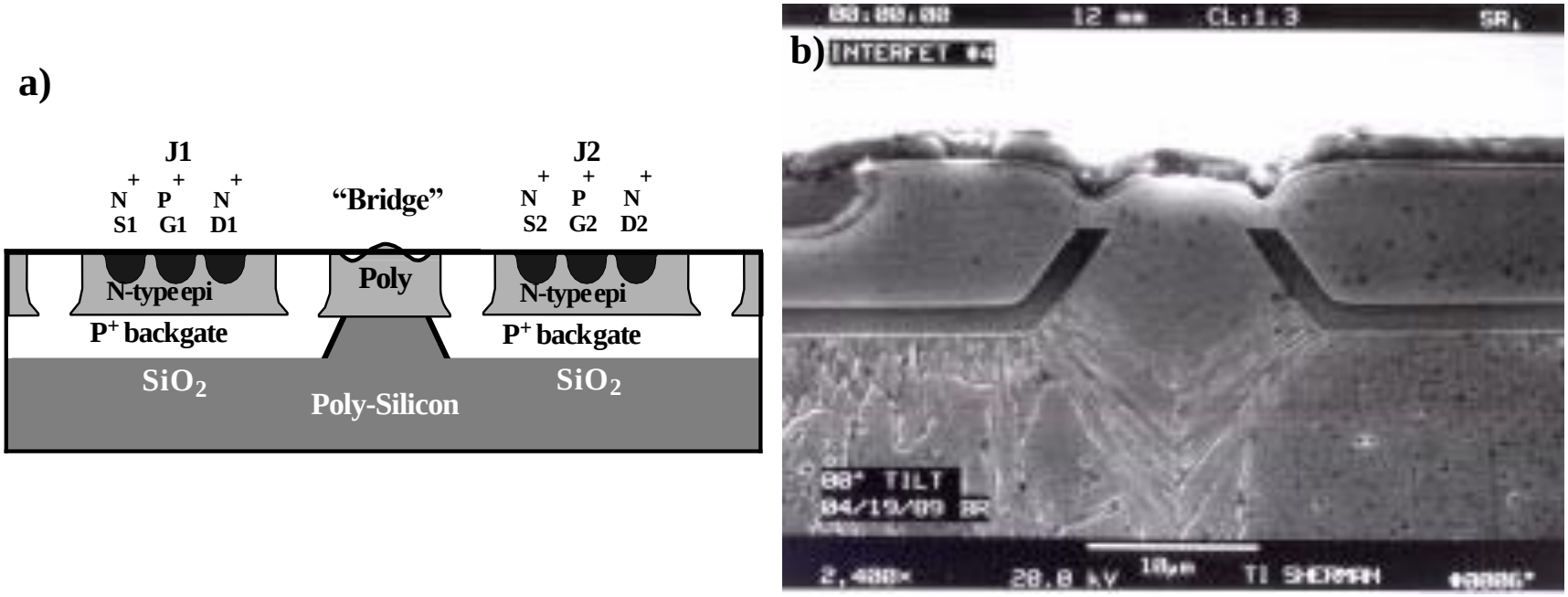
An extensive U.S. Department of Energy review was done during the mid-1980s. Seventeen shafts were sunk and 23.5 km (14.6 mi) of tunnel were bored by late 1993.[3][9]

The Monolithic JFET Process Project

- First we tried simply to work with Interfet to build larger JFETs (NJ450, NJ903, NJ1800, NJ3600)
- Based on our collective experience we soon thought to exploit the low noise properties, rad hardness, cryogenic capabilities of JFET to build a monolithic preamplifier
- Interfet (a spin-off of Texas Instruments) had access to Ti Simox material, and ….



Dielectric Isolation Process

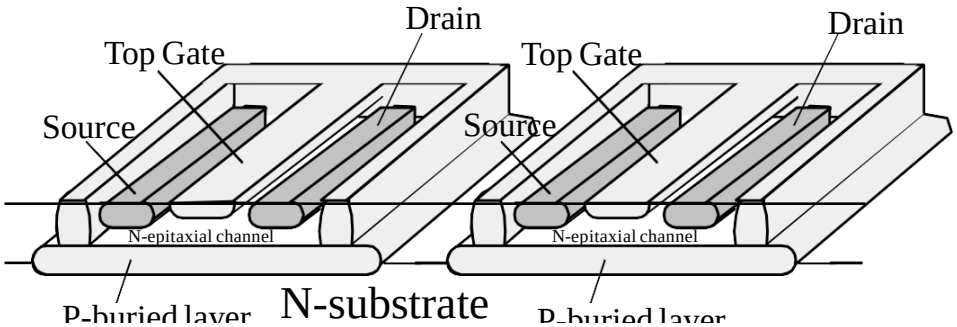


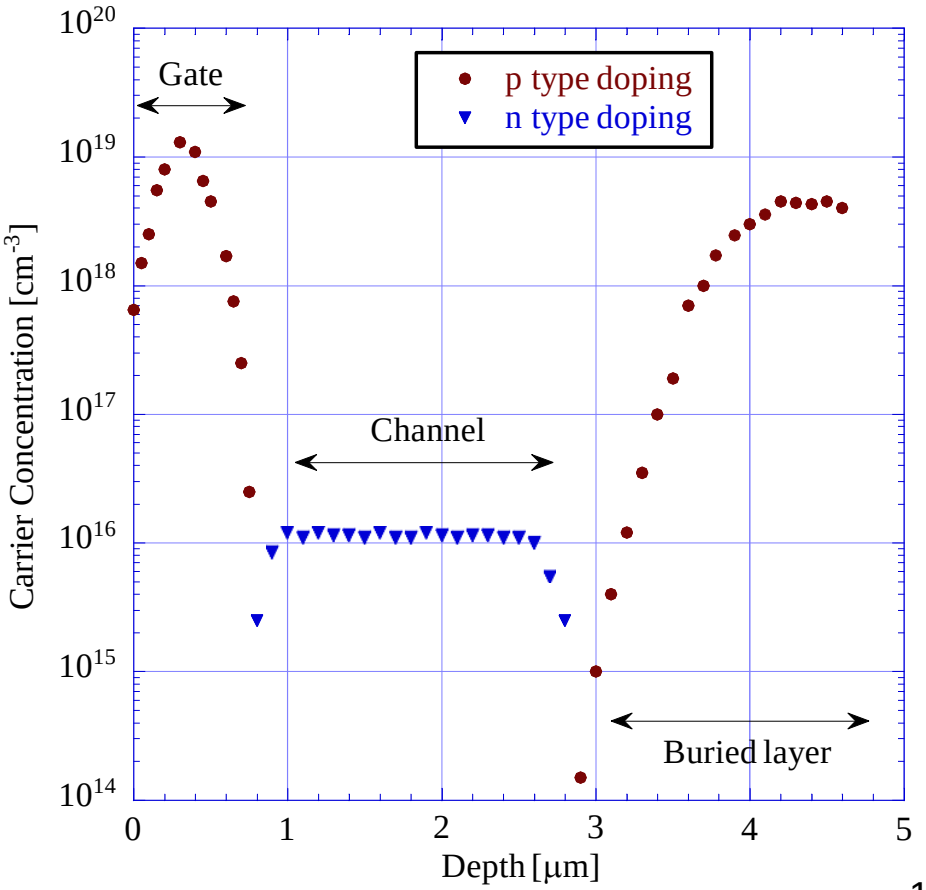
Dielectric isolation process devices.

a): Devices built in adjacent tubs are connected by back to back diodes in series with a high value resistor due to the polysilicon bridge shown in b).
If true isolation is needed, anisotropic etching can be employed to leave free standing "mesas" of silicon on a SiO2 floor.

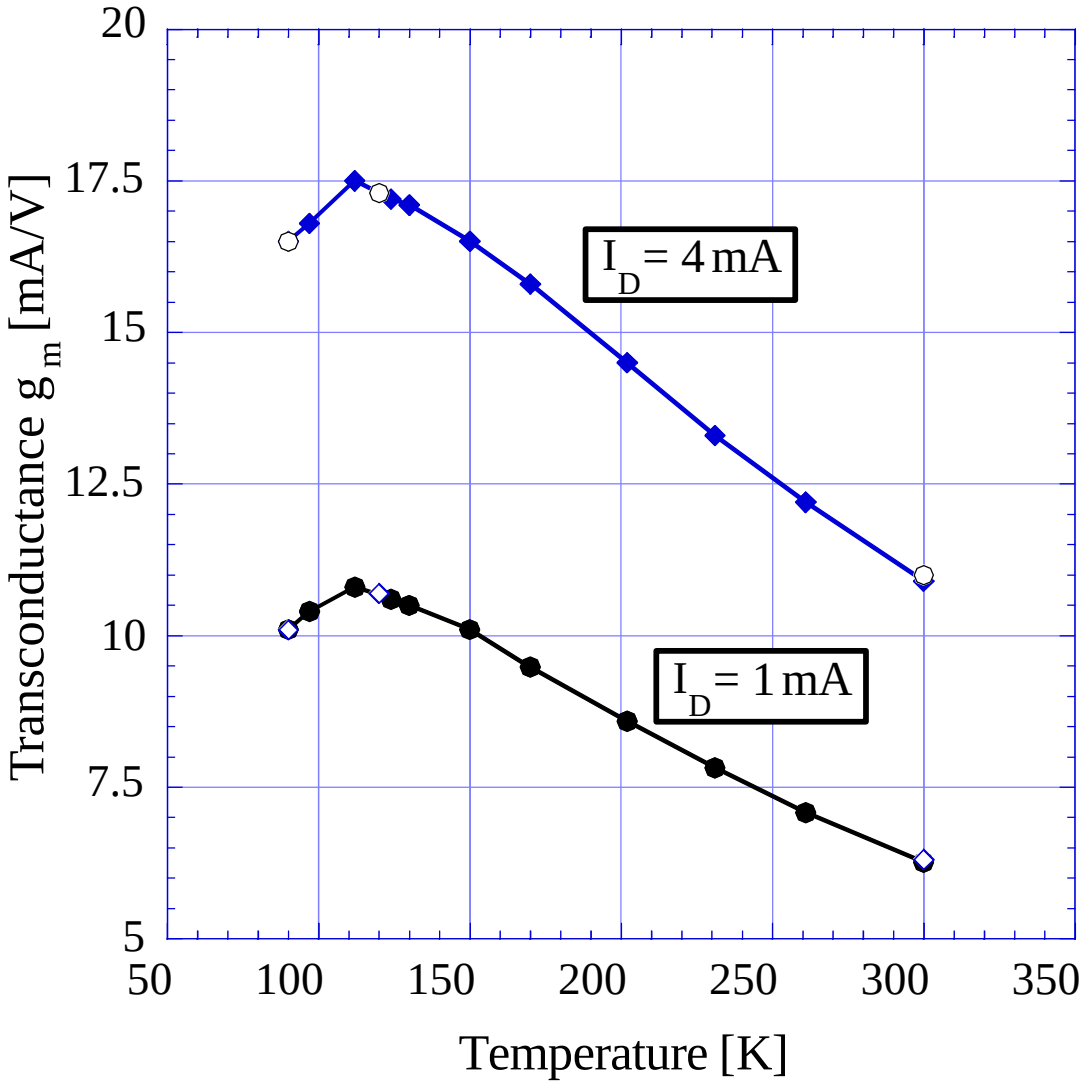
BURIED LAYER PROCESS

1	Starting wafer: 0.5 Ωcm, N-type, (111) Silicon
2	Diffuse back-gate wells: 0.002 Ωcm
3	Grow oxide: t_{ox} ~ 50 nm
4	Strip oxide, chemical clean and epi growth. t_{epi} ~ 5-7 μm R_{epi} = 0.5 Ωcm (L-type) and 1.5 Ωcm (H-type)
5	Pattern and diffuse isolation ring (P-type)
6	Pattern gate and gate diffusion (P-type)
7	Pattern source and drain and diffusion (N-type)
8	Open contact window. Probe test structures. Gate targeting (by additional drive-in)
9	Nitride deposition (dielectric layer to isolate metal)
10	Evaporate and pattern metal (aluminum)
11	Nitride protective overcoat



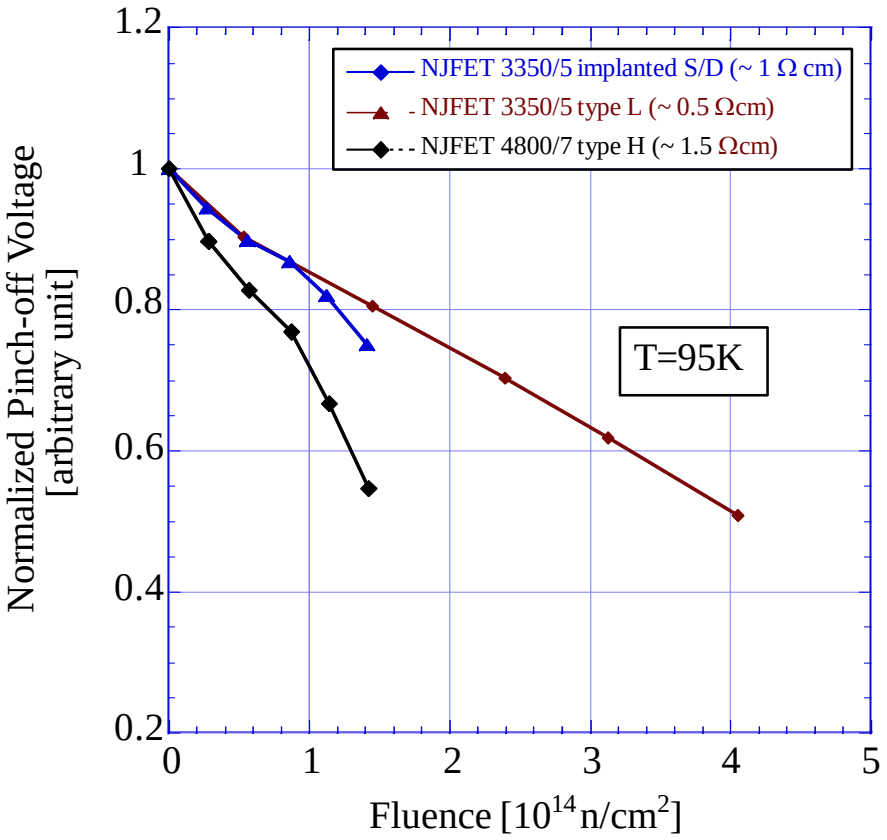


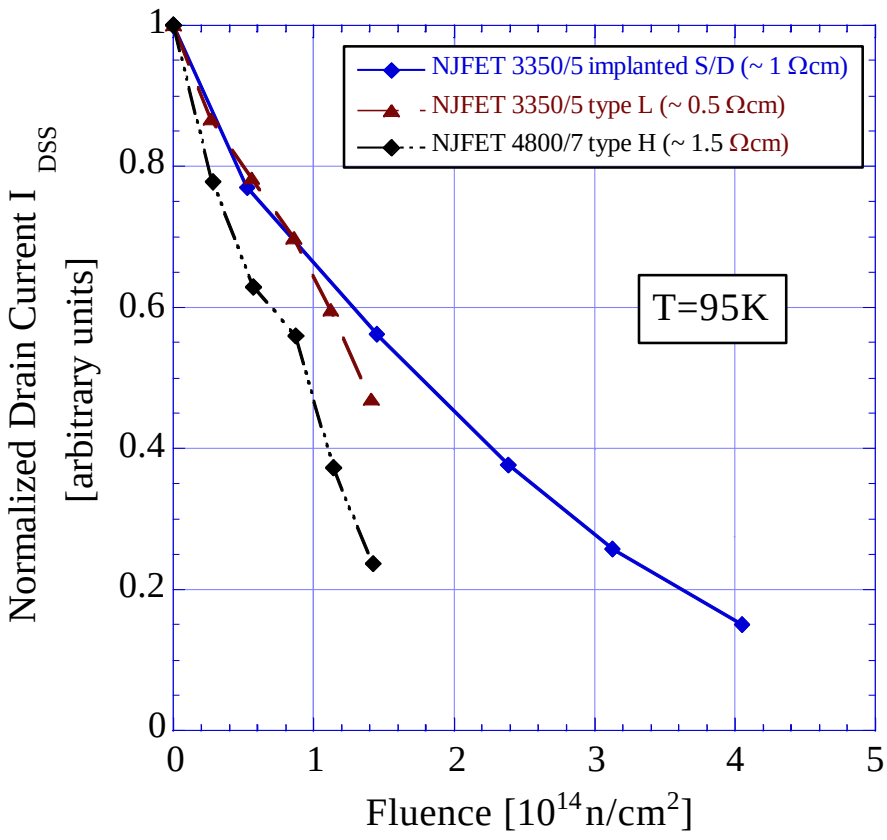
TEMPERATURE DEPENDENCE (55Mrad)



Temperature dependence of the transconductance g_m before (white symbols) and after (solid black symbols) a 55 Mrad γ-ray irradiation for an implanted NJFET (W/L = 2500/5) in the saturation region (VDS = 2.5 V).

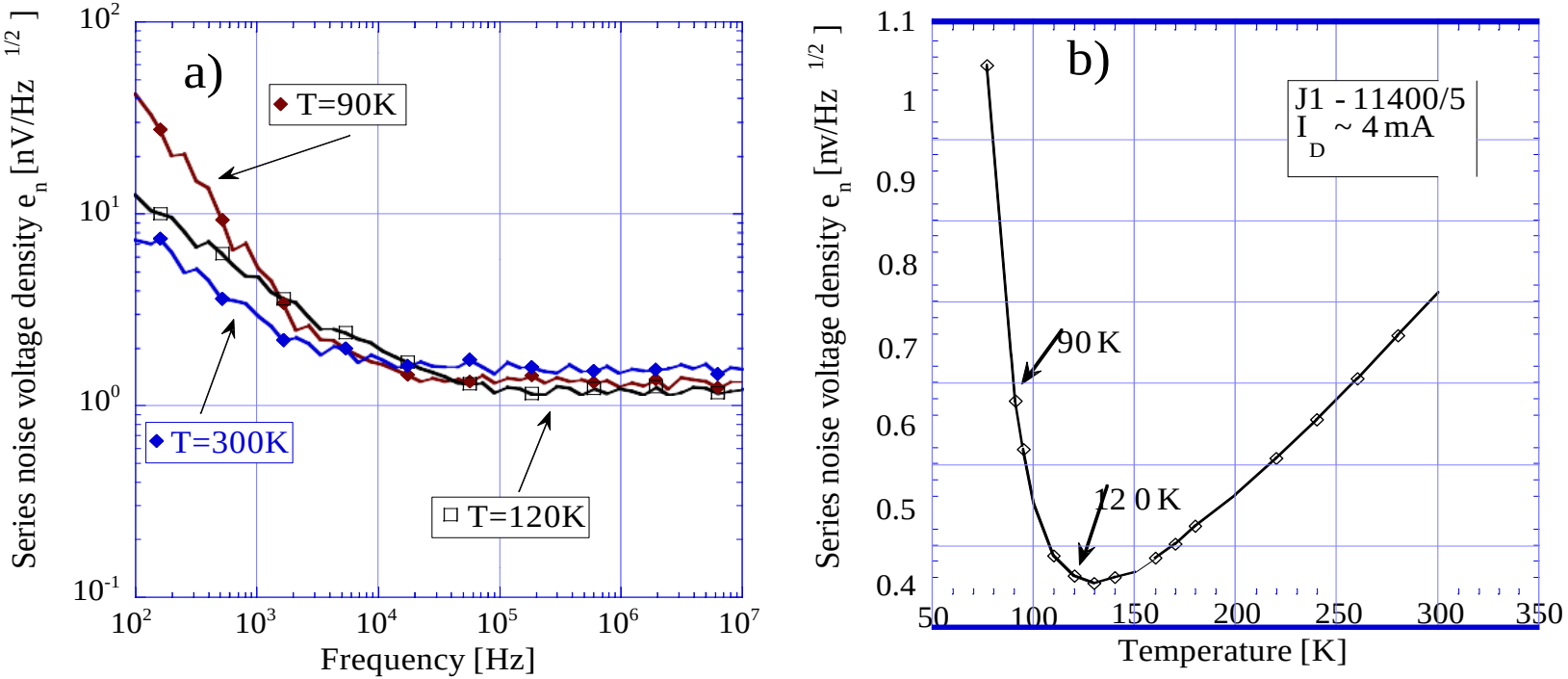
Neutron Damage: V_p and IDSS





Pinch-off voltage and drain current IDSS (VGS = 0) as a function of neutron fluence at a constant temperature of 95 K for devices of different channel resistivities. The curves have been normalized to the pre-irradiation values. The transistors have been irradiated and measured in the saturation region (VDS = 2.5 V) at T = 95 K.

Noise vs Temperature



Noise characteristics vs. temperature. (a): Series noise voltage density at 300 K, 120 K and 90 K for an unirradiated monolithic H-type NJFET (W/L = 2800/5). The transistor has been measured in the saturation region with V_{DS} = 2.5 V and I_D = 1 mA. (b): Temperature dependence for the high frequency component (white noise) of the series noise voltage density of a preamplifier whose input device is a monolithic H-type NJFET (W/L = 11400/5). The e_n values have been obtained from equivalent noise charge measurements. The input transistor was operating in the saturation region with a standing current I_D = 4 mA at room temperature.

Noise vs γ Irradiation (55Mrad)

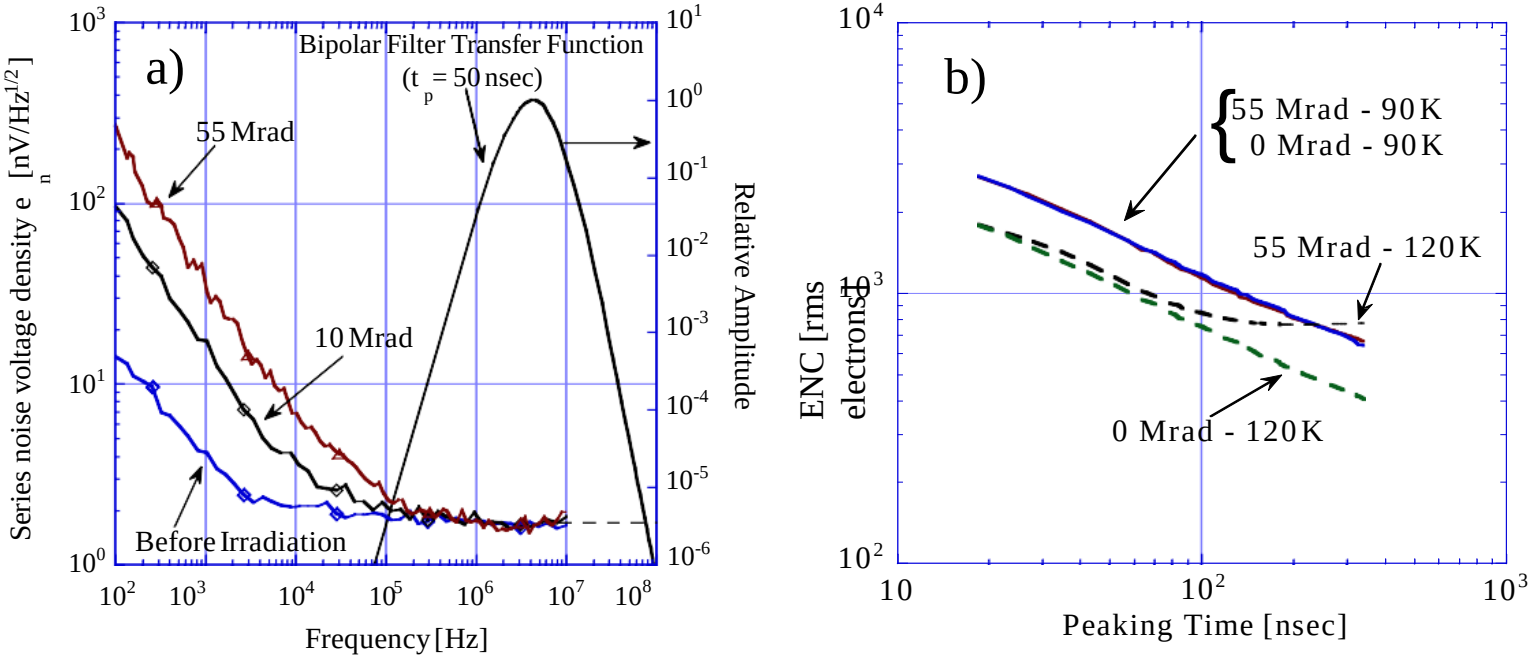


Figure 3-16. γ-ray induced effect on noise. (a): Series noise voltage density after various doses of ^{60}Co γ-ray radiation at a constant temperature of 90 K for an implanted NJFET (W/L = 2500/3). The transistor has been irradiated and measured in the saturation region (V_{DS} = 2.5 V, I_D = 1 mA) at 90 K. A bipolar filter transfer function (t_p = 50 nsec) has been superimposed to the e_n values to highlight the frequency region of interest for liquid ionization calorimetry. (b): Computed equivalent noise charge (ENC) at 90 K and 120 K before and after irradiation (55 Mrad). The 90 K noise densities are the ones of (a). The calculation assumes a C_{ISS} ~ 11 pF, C_D = 33 pF, no parallel noise contribution and a CR^2-RC^2 bipolar filter transfer function.

Noise vs neutron irradiation (4E14n/cm^2)

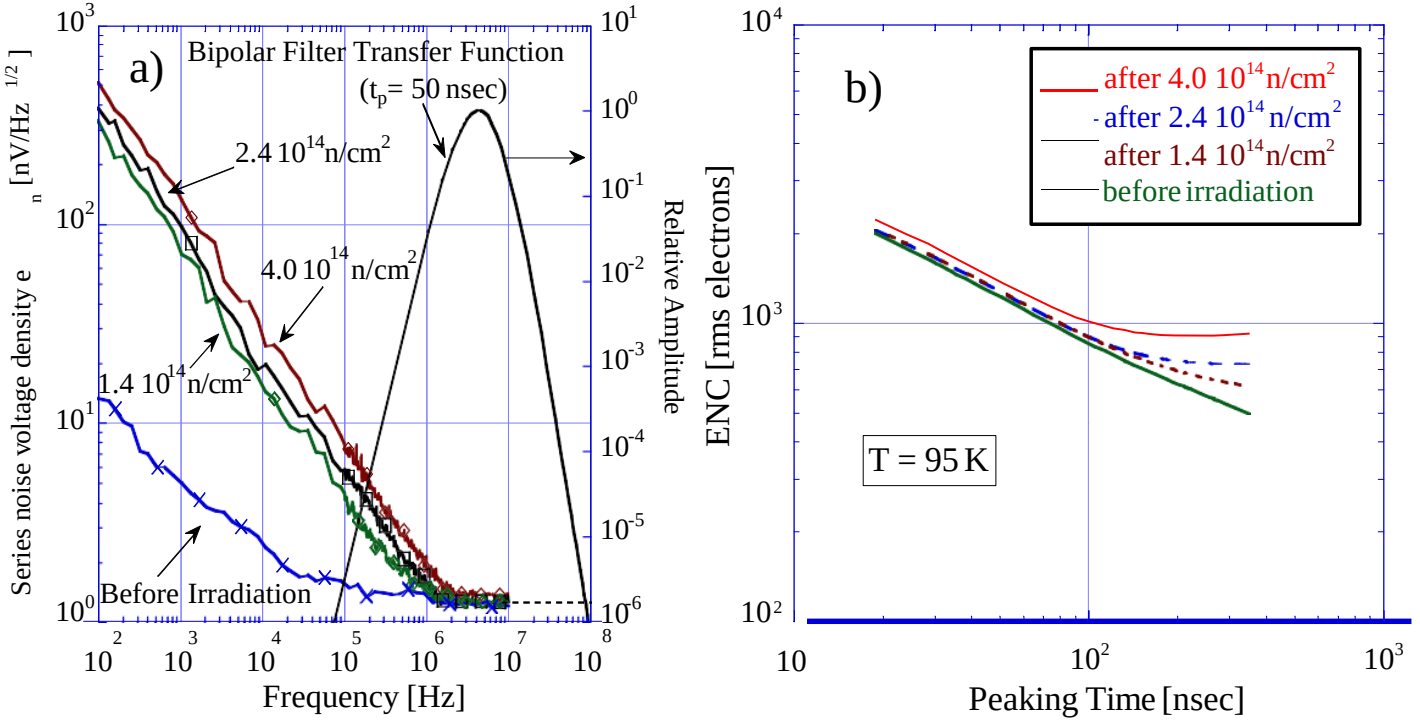


Figure 3-17. Neutron irradiation effects on noise. (a): Series noise voltage density after various neutron fluences at a constant temperature of 95 K for an implanted NJFET (W/L = 3350/3). The transistor has been irradiated and measured in the saturation region (V_{DS} = 2.5 V, I_D = 1 mA) at 95 K. A bipolar filter transfer function (t_p = 50 nsec) has been superimposed to the e_n values to highlight the frequency region of interest for liquid ionization calorimetry. (b): Computed equivalent noise charge (ENC) at 95 K after various neutron fluences using the series noise voltage density of (a). The calculation assumes a NJFET (W/L = 3350/3) with a C_{ISS} ~ 15 pF, C_D = 33 pF, no parallel noise contribution and a CR^2-RC^2 bipolar filter transfer function.

IPA3 Monolithic JFET Preamplifier

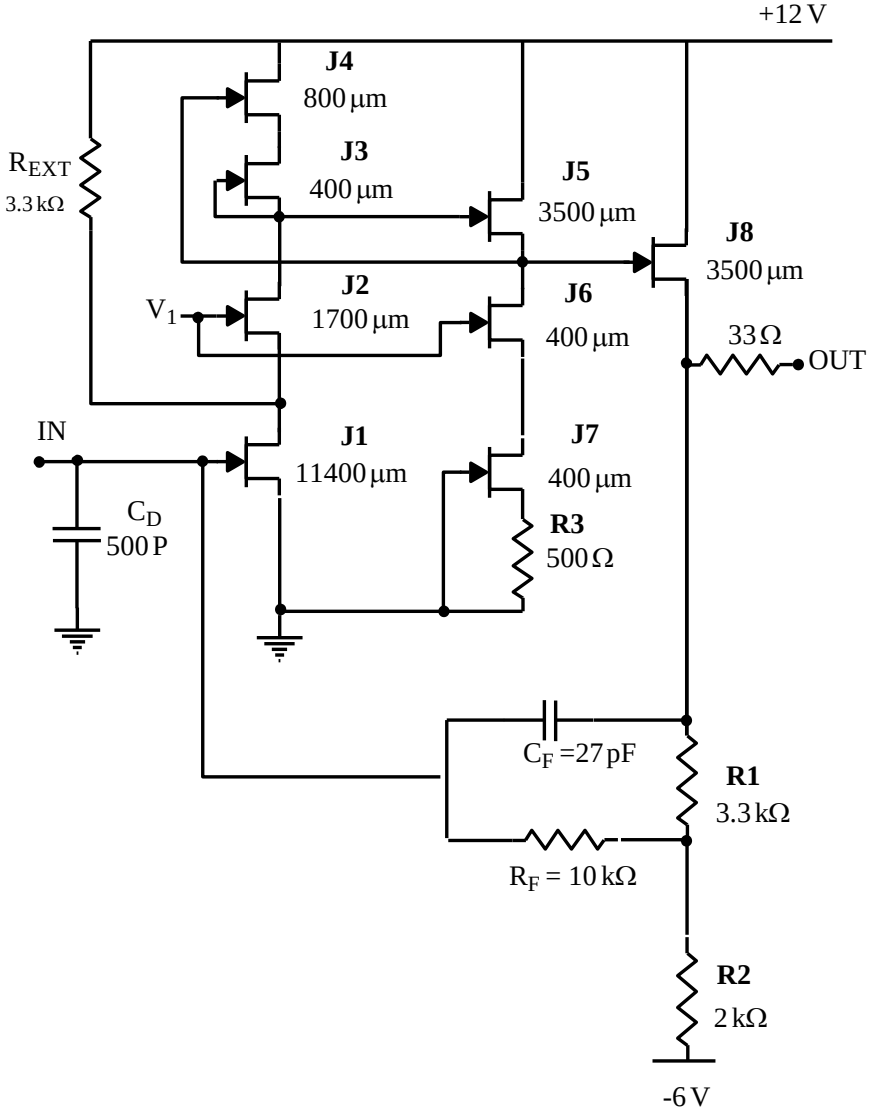
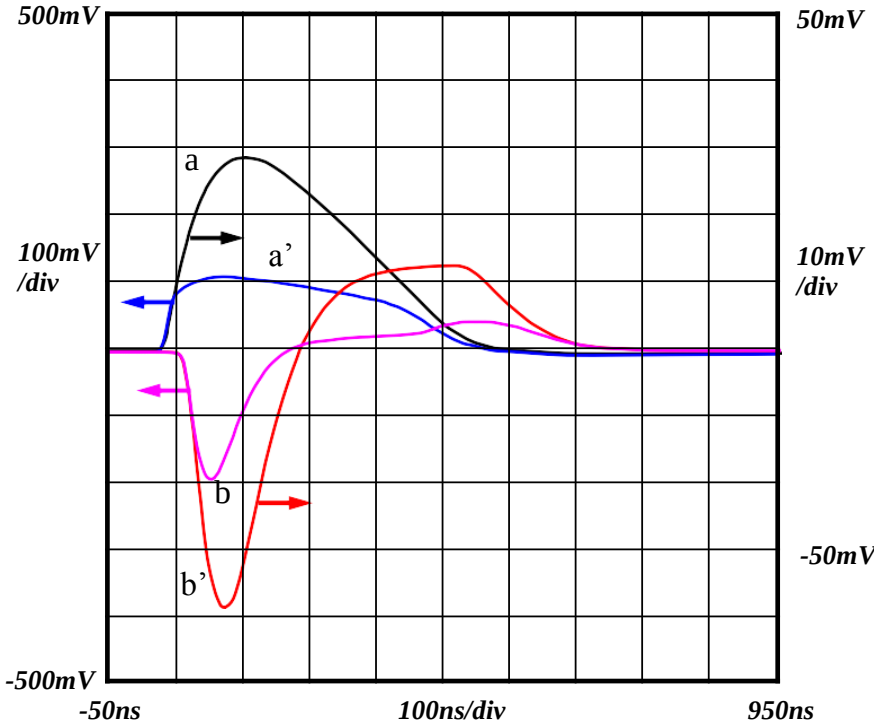


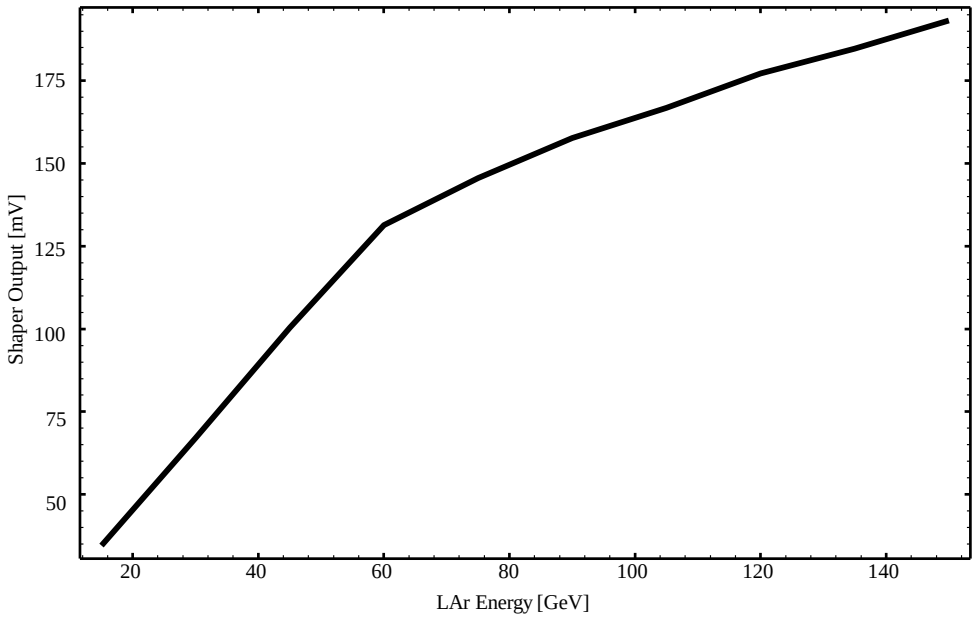
Figure 3-20. IPA3 version of the preamplifier built by means of the buried layer, epitaxial channel monolithic JFET technology. Only the active elements are monolithically integrated. All resistors and capacitors were external discrete components.

IPA3 Monolithic JFET Preamplifier Measured Characteristics

Parameter		L-type	H-type
Input Device		NJFET, W = 11400 μm, L = 5 μm	
Open-loop input capacitance		50 pF	40 pF
Power dissipation		80 mW	
DC gain A_0	Z_{OUT} = 10 kΩ	82 dB	75 dB
	Z_{OUT} = 100 Ω	76 dB	70 dB
Rise time (C_D = 500 p, C_F = 33 pF)		15 ns	
Noise voltage /√Hz] (f > 1 kHz)	T= 300 K	0.6	0.7
	T = 120 K	0.4	0.4
Equivalent noise charge [e rms] $(RC)^2$ -$(CR)^2$ bipolar shaping at t_p = 50 ns		ENC = 1200 + 18 C_D	ENC= 1100+ 21 C_D

Bilinear Characteristics





Time domain response of the output of the IO751 bi-linear preamplifier in the linear and non linear regions after the preamplifier (curves a, a') and after shaping (curves b, b') at t_p = 50 ns. The input currents correspond to a LKr energy of 15 GeV (curves a and b) and 150 GeV (curves a' and b') and the vertical scales are also scaled by a factor of ten.

Bi-linear transfer characteristics from LAr in to peak shaper out for the IO751 preamplifier. The break point is at 60 GeV, and the ratio of the two slopes is about 4.

1993: Abrupt SSC Cancellation

- The R&D was quickly terminated.
  Yet to do:
  - Monolithic Resistors
  - Monolithic Capacitors
  - Discharge Protection

- … but a rich heritage:

- Very low noise audio hearing aid
- Very large JFET Development
- Proof of Principle of 10s of Mrad Radiation Hardness
  (one preamp was irradiated to 300Mrad, still working)

PHYSICS BASEL
ELECTRONIC LAB MICHAEL
STEINACHER
KLINGELBERGSTR. 82
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SWITZERLAND

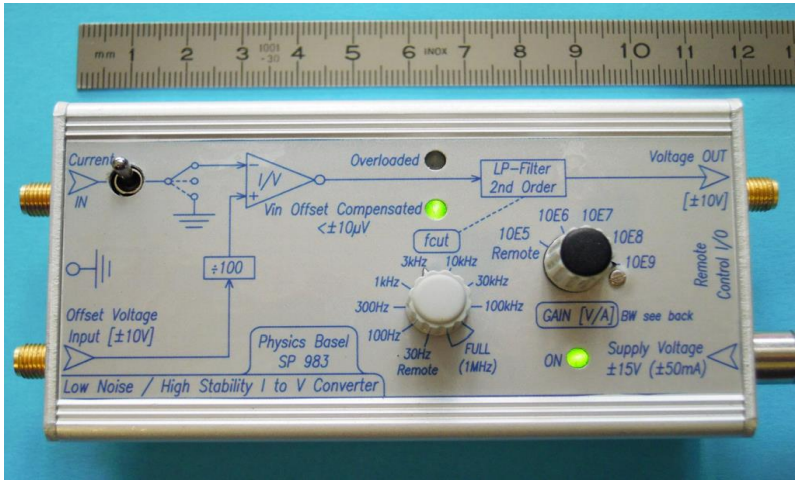
LOW NOISE / HIGH STABILITY I TO V CONVERTER

SP 983 WITH IF3602

DATASHEET VERSION 1.2

SEPTEMBER 2014

FEATURES



- Low input voltage noise
  → Typical input referred voltage noise: 2 nV/sqrt(Hz) @ 10 Hz
  1.2 nV/sqrt(Hz) @ 1 kHz
- Stable and low drift input voltage
  → Typical input voltage drift @25°C:
  ±0.15 µV/K
- Input current noise level:
  → 6.1 fA/sqrt(Hz) @10 Hz, 10^9 V/A
- Five decades of gain: 10^5…10^9 V/A
- Broadband (e.g. min. 20 kHz @ 10^8 V/A)
- Integrated low-pass-filter: 30 Hz…100 kHz
- Remote controllable gain and LP-cutoff
- Input voltage can be shifted up to ±100 mV by an external offset voltage
- Green LED indicates when input offset voltage is compensated and stable
- Red LED indicates overloaded condition
- SMA input & output connectors / BNC-adapters included
- Overload protected current input

Franco's 200pV/√Hz amplifier: World Record?

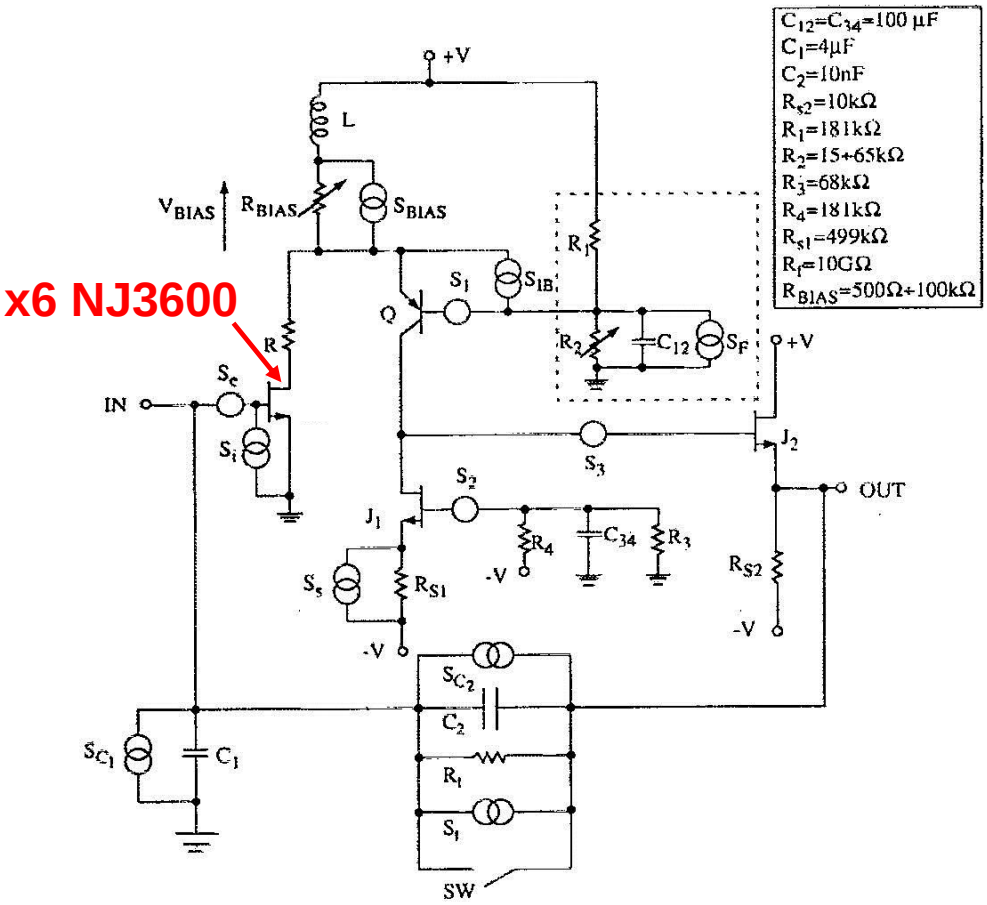


FIG. 2. Detailed schematic of the front-end unit.

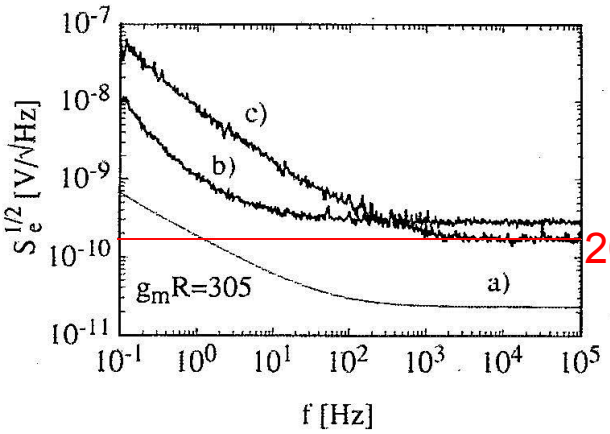
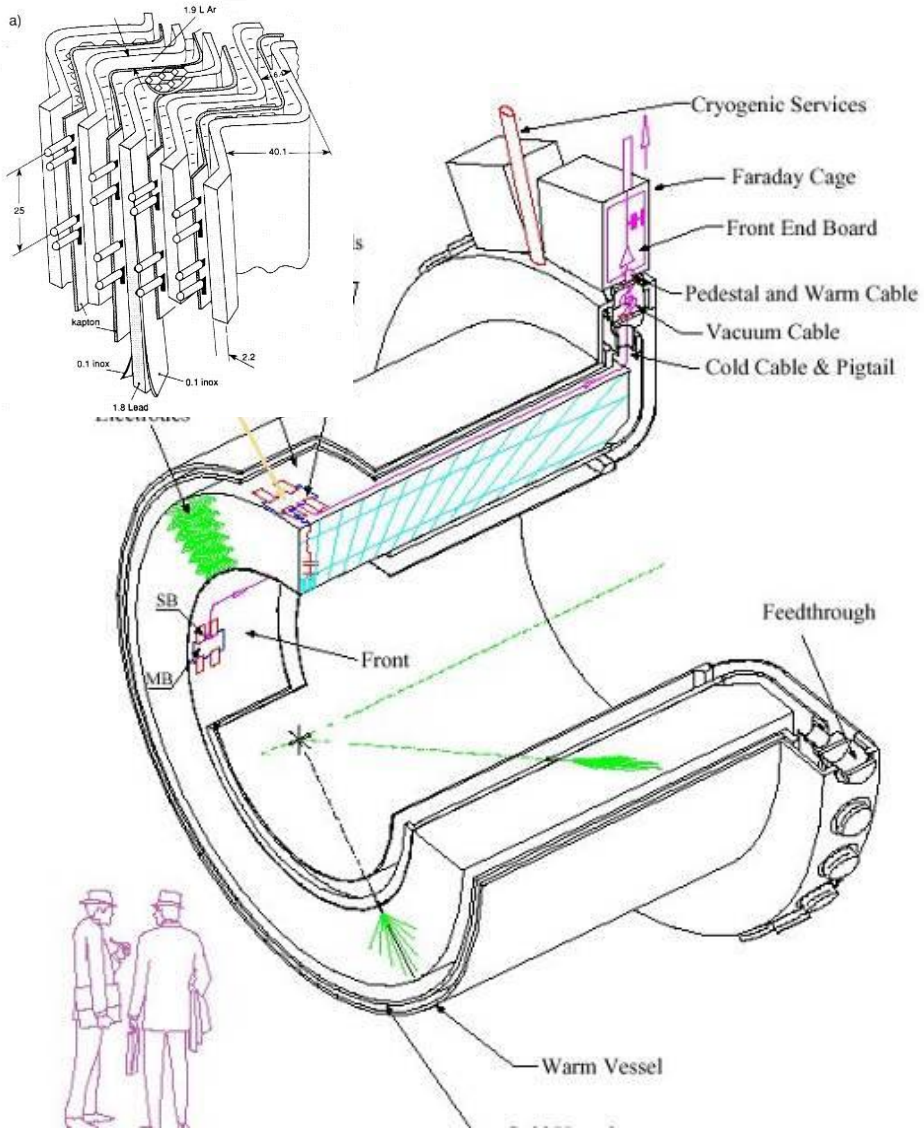


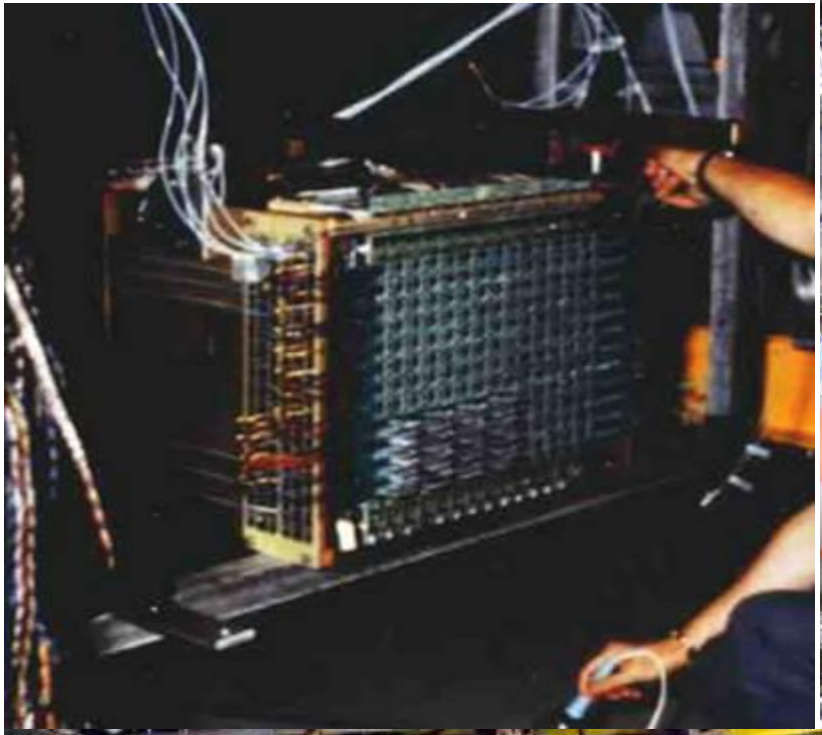
FIG. 4. Square root of the noise power density $S_e(f)$ as a function of frequency. a) Calculated contribution which adds quadratically to the noise voltage of the DUT as a combined effect of the noise in all the other active and passive components in the front-end unit. b) Square root of spectral noise density measured on the parallel combination of six JFETs working at a total standing current of 2.5 mA. c) Square root of spectral noise density measured on the same combination of JFETs at a total standing current of 28.7 mA.

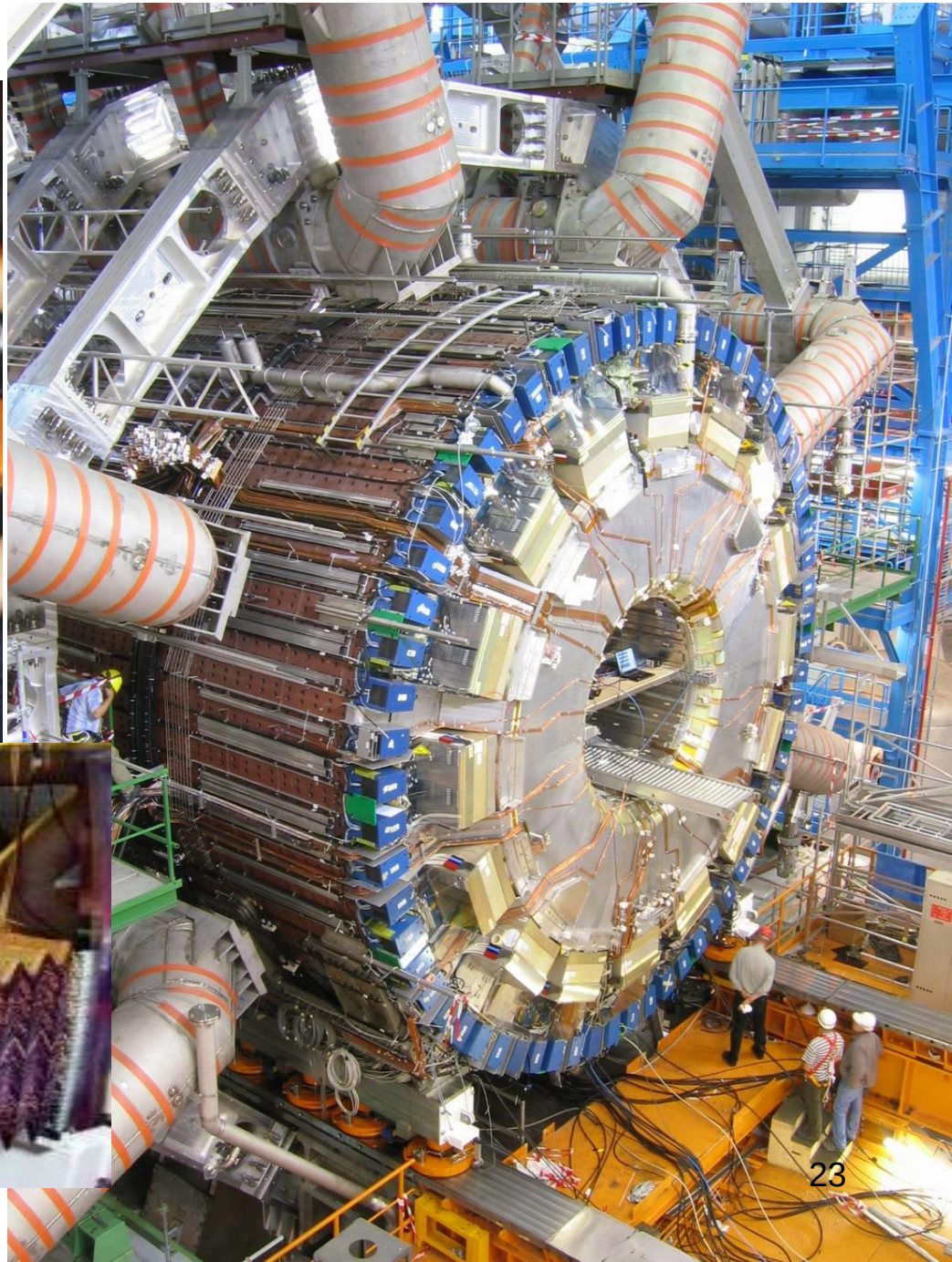
LHC ATLAS Calorimeter (1990s-2000s)

- Challenging LHC
  - High energy 14 TeV
  - High collision rate : 40 MHz
  - Small branching ratios…
- Challenging calorimetry
  - Good resolution
  - Small constant term (<1%)
  - Low dead material
- Challenging electronics
  - Large dynamic range (16 bits)
  - Low noise
  - High speed
  - High radiation hardness
- Challenging schedule
  - Be ready for 1999 !



ATLAS @ LHC

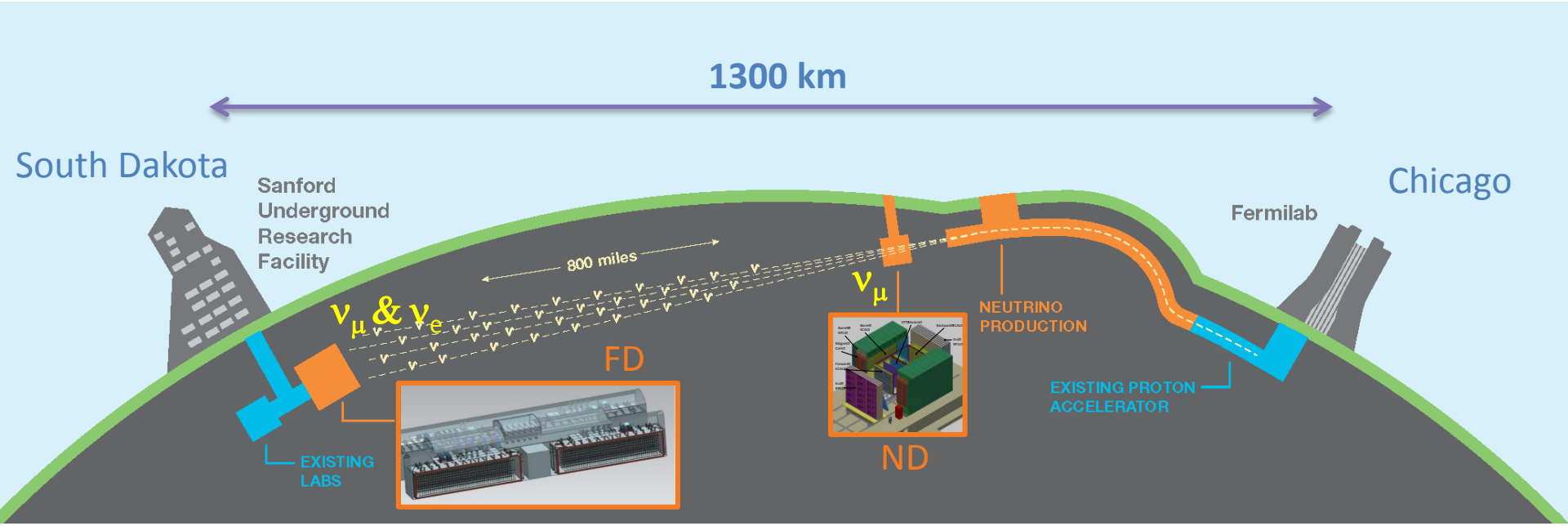




DUNE neutrino Experiment (Lar)

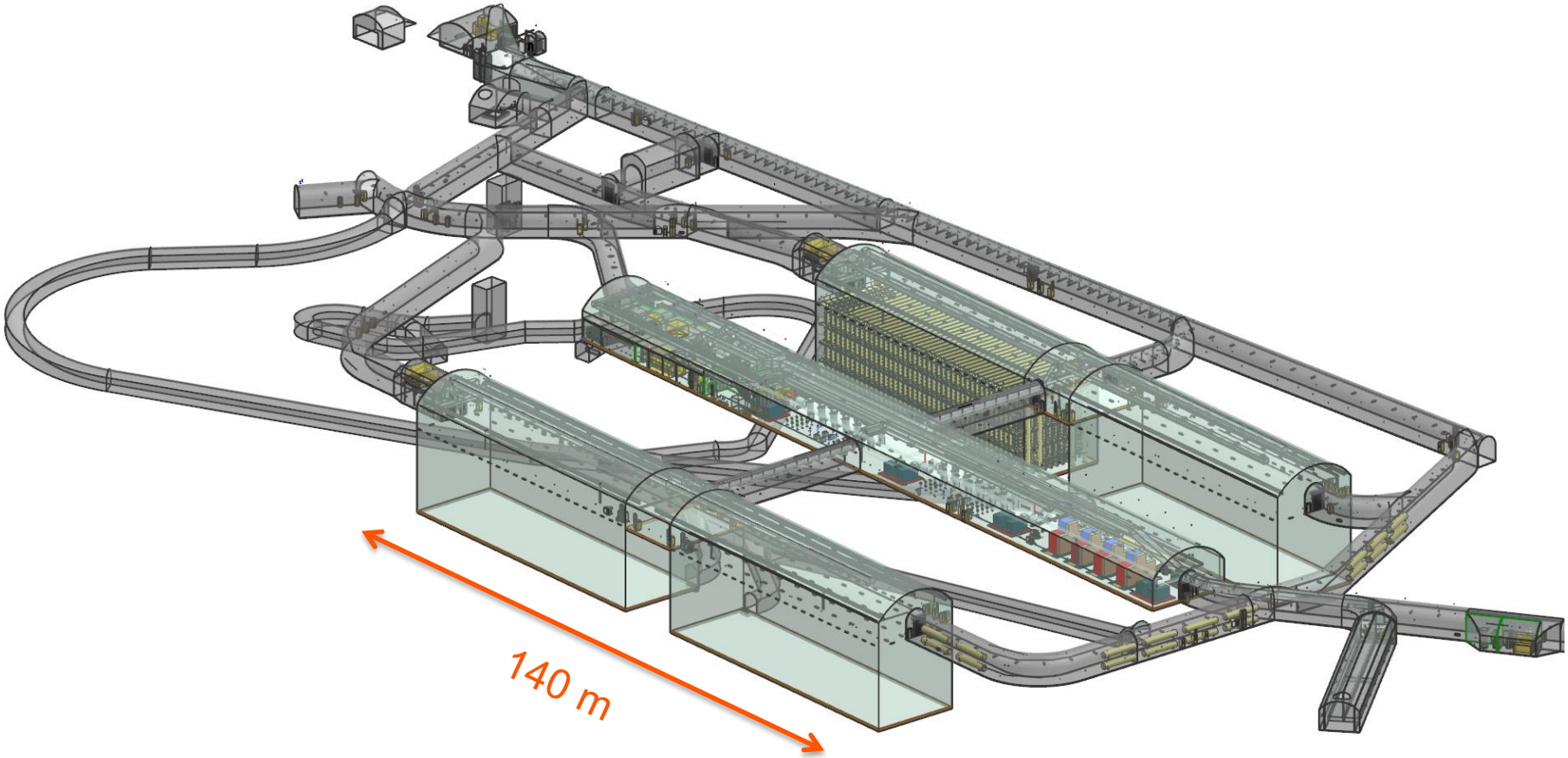
★LBNF/DUNE

- Muon neutrinos/antineutrinos from high-power proton beam
  - **1.2 MW** from day one (upgradeable)
- Large underground **Liquid Argon Time Projection Chamber**
  - **4 x 17 kton ➡ fiducial (useable) mass of >40 kton**
- Near detector to characterize the beam



DUNE Design =

- **Far detector:** **70-kt LAr-TPC = 4 x 17 kt detectors**



THE LHC LUMINOSITY MONITOR

THE CONCEPT WHICH UNDERLIES THE LUMINOSITY MONITOR FOR LHC

Proton-proton collisions at the Interaction Points (IP) of (LHC) will produce high fluxes of neutrons and photons that will be intercepted by the neutral absorbers located about 140m downstream the IP1 and IP5 collision points. ***The energy associated with the showers initiated by the neutral flux from the IPs is proportional to the charge of the colliding bunches and hence to the luminosity.***

The study was focused on a detector able to provide information on the shower population with response times compatible with the 40 MHz bunch collision frequency.

The idea was to install it into a slot machined inside the copper core of the absorbers in order to monitor and optimize the LHC luminosity in a bunch-by- bunch operation.

The first problem was identifying the detector type suitable for the purpose. The luminosity monitor is a nearly zero-angle detector and as such it will be exposed to an extremely high dose of radiation. It should stand, before a replacement is possible, up to 1 GGy, a dose exceeding by at least two orders of magnitude that expected for detectors in LHC experiments. Ordinary solid-state detectors were discarded as it was concluded that they wouldn't survive long enough for the purpose. Polycrystalline CdTe was proven to be promising, but later it was abandoned because of technological difficulties in the realization of adequately large sensitive areas. The best solution was identified to be a multigap ionization chamber operating at a high pressure of the filling gas.

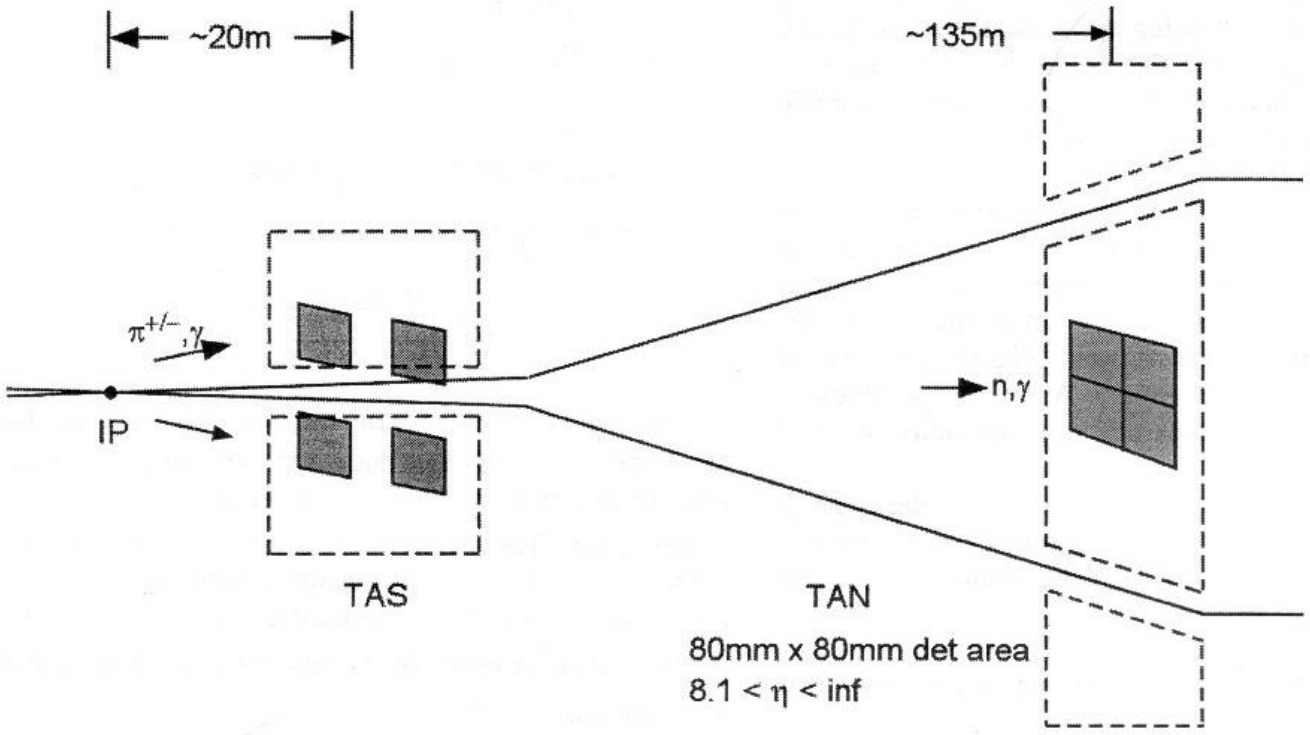


Fig. 4: Illustration of ionization chamber detectors in the TAN and TAS absorbers.

DETECTOR EVOLUTION

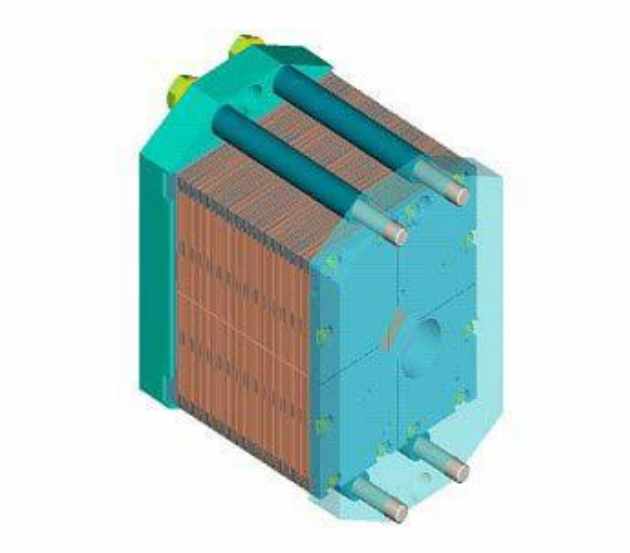
First version (years 2000, 2001)

$N_{GAP} = N_{SER} \times N_{PAR} = 60$

$x_{GAP} = 0.5$ mm

drift vel. = 3 cm/μs (98% Ar + 2% N_2)

$C_{DETECTOR} = C_{GAP} \times N_{PAR} / N_{SER}$



Second version (years 2003 e 2004)

$N_{GAP} = N_{PAR} = 6$

$x_{GAP} = 1$ mm

drift vel. = 4.5 cm/μs (94% Ar + 6% N_2)

Q_{GAP} doubled

C_{GAP} halved

$C_{DETECTOR} = C_{GAP} \times N_{PAR}$

Remembering Franco

- A wonderful, knowledgeable and patient teacher. A sad loss, for his family, his colleagues, his friends and the scientific community.
- “The end of an era…”
- Having studied with him, worked with him, had fun with him, he has enriched my life, the lives of all of us and set an example on how to balance life and career.

From Veljko Radeka:

Remembering Franco ….

I met Franco a little more than half a century ago.

This gave me a lasting feeling of the warmth of an extraordinary human being, whether when we got together , or only when exchanging brief messages.

He succeeded in being magnanimous and supportive to others while having to deal with some untimely losses suffered by his family.

His patience in life was also evident in the approach to his work, always a very careful and thorough analysis, and even in his lecture notes in his exceptionally neat handwriting …

For many years I received a message from Franco for Thanksgiving Holiday.

Last year there was no message ….

I will always remember my dear friend,

Veljko

A small sample of Franco's work:

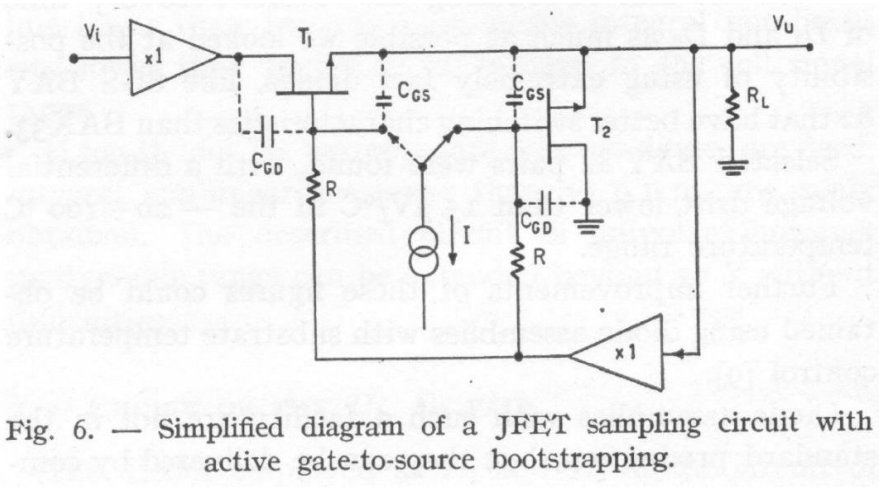


Fig. 6. — Simplified diagram of a JFET sampling circuit with active gate-to-source bootstrapping.

From: Alta Frequenza, Vol XI, 1971

Franco was fascinated by JFETs
Above: A precursor to MOS switched capacitor circuits …